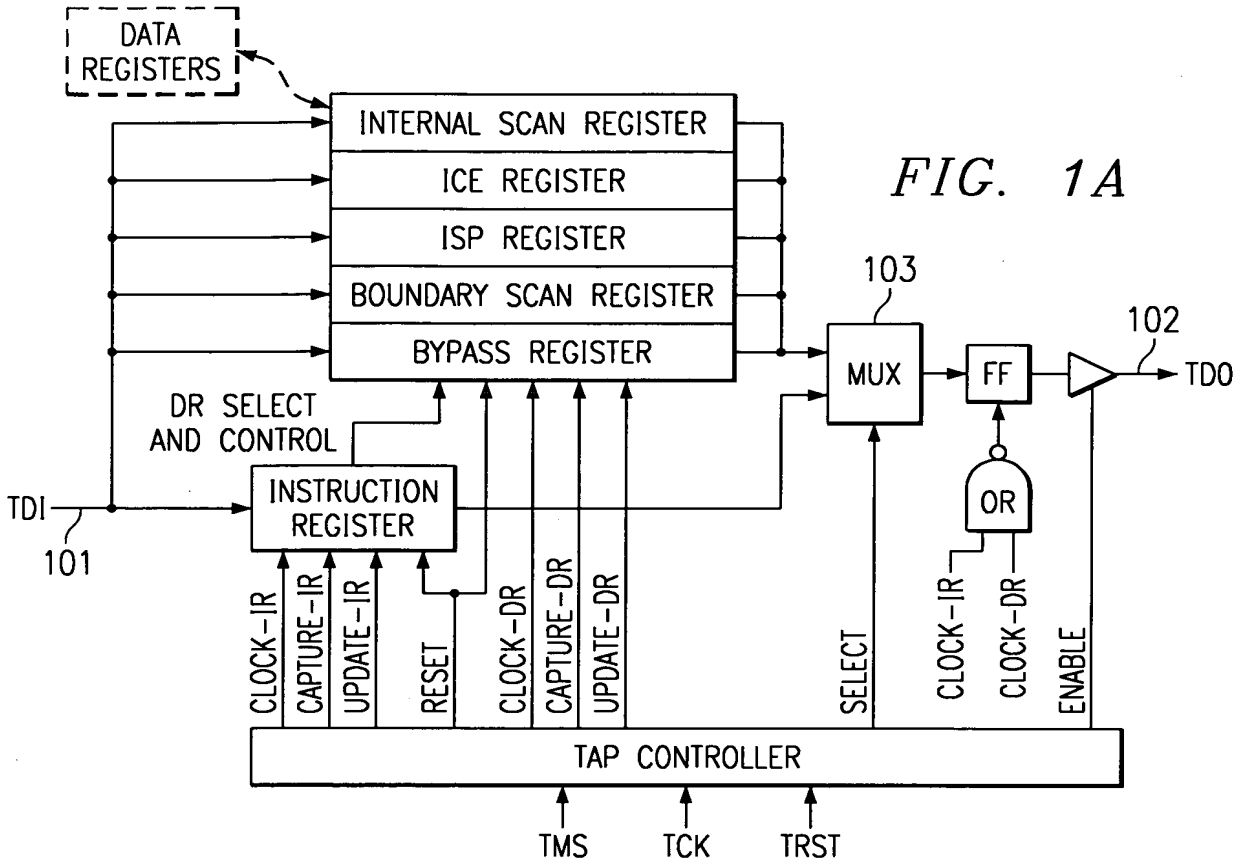
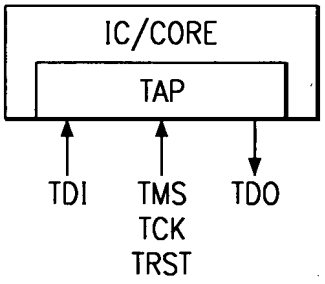


FIG. 1A

FIG. 1B



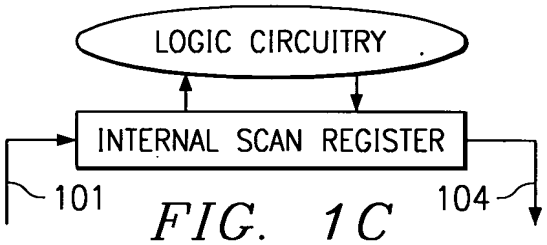


FIG. 1C

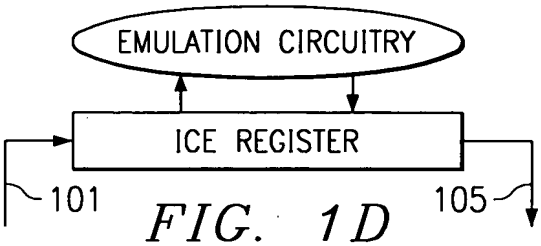


FIG. 1D

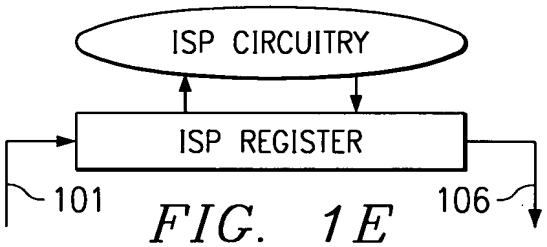


FIG. 1E

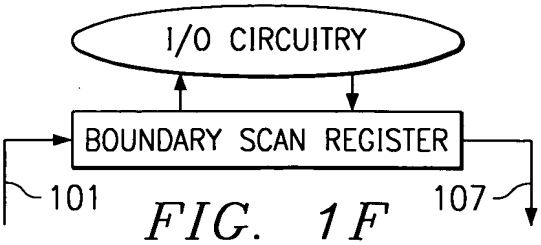


FIG. 1F

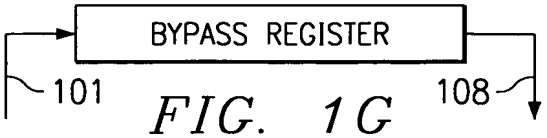


FIG. 1G

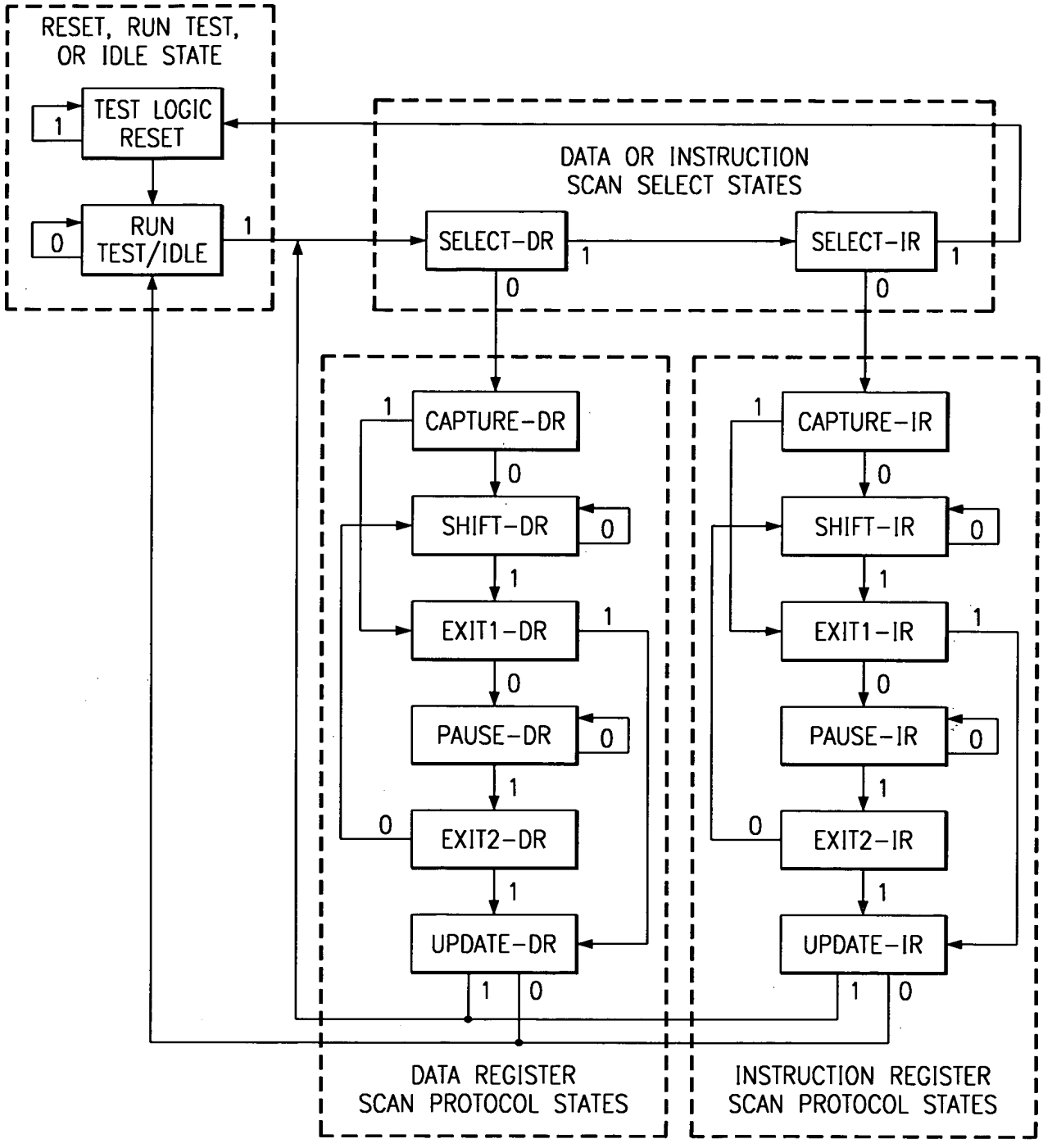

RESET, RUN TEST,
OR IDLE STATE
TEST LOGIC
RESET
RUN
TEST/IDLE
DATA OR INSTRUCTION
SCAN SELECT STATES
SELECT-DR
SELECT-IR
CAPTURE-DR
SHIFT-DR
EXIT1-DR
PAUSE-DR
EXIT2-DR
UPDATE-DR
CAPTURE-IR
SHIFT-IR
EXIT1-IR
PAUSE-IR
EXIT2-IR
UPDATE-IR
DATA REGISTER
SCAN PROTOCOL STATES
INSTRUCTION REGISTER
SCAN PROTOCOL STATES

FIG. 2

FIG. 3A

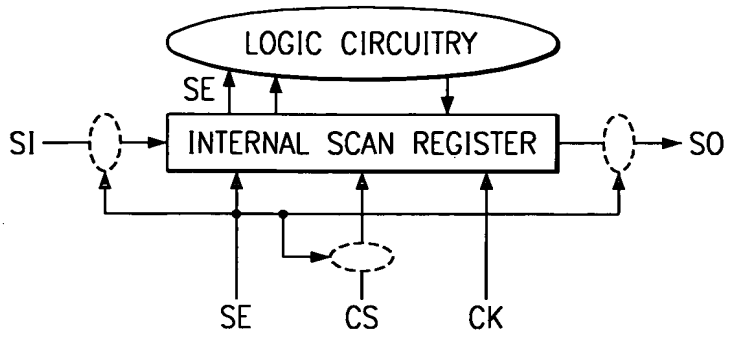


FIG. 3B

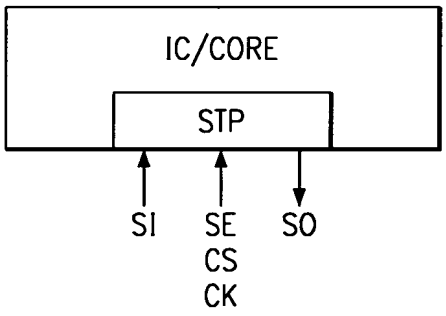
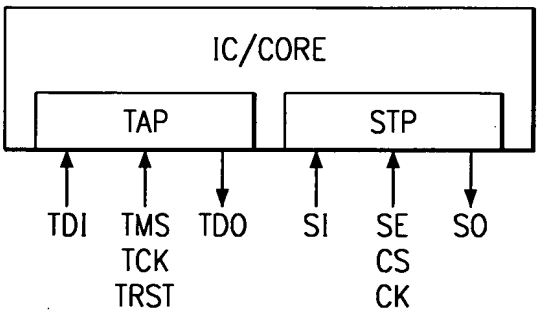


FIG. 3C



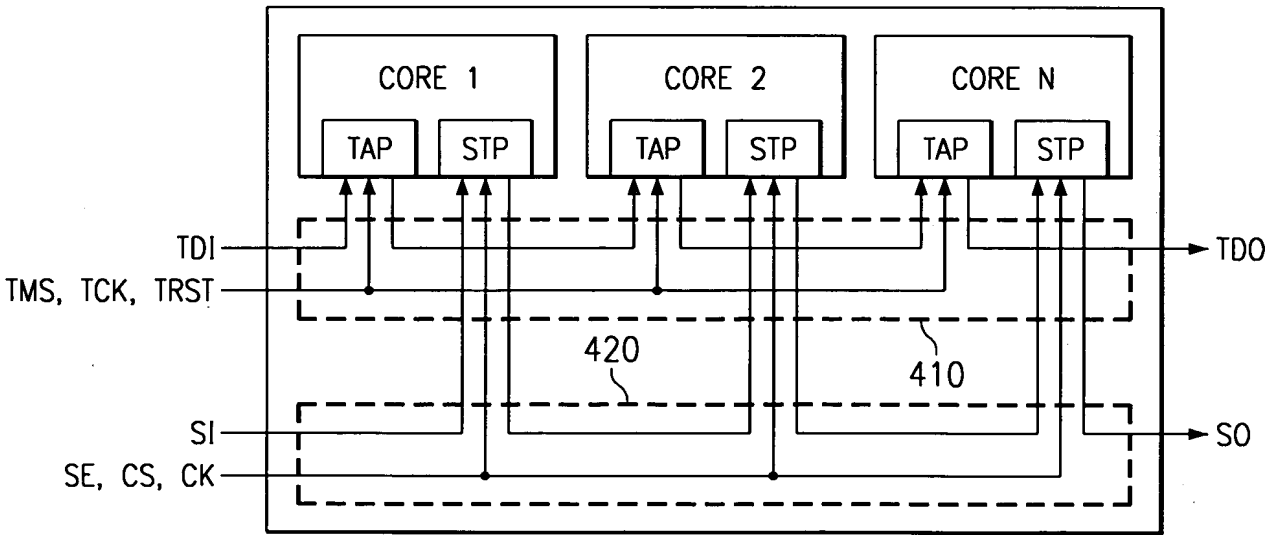
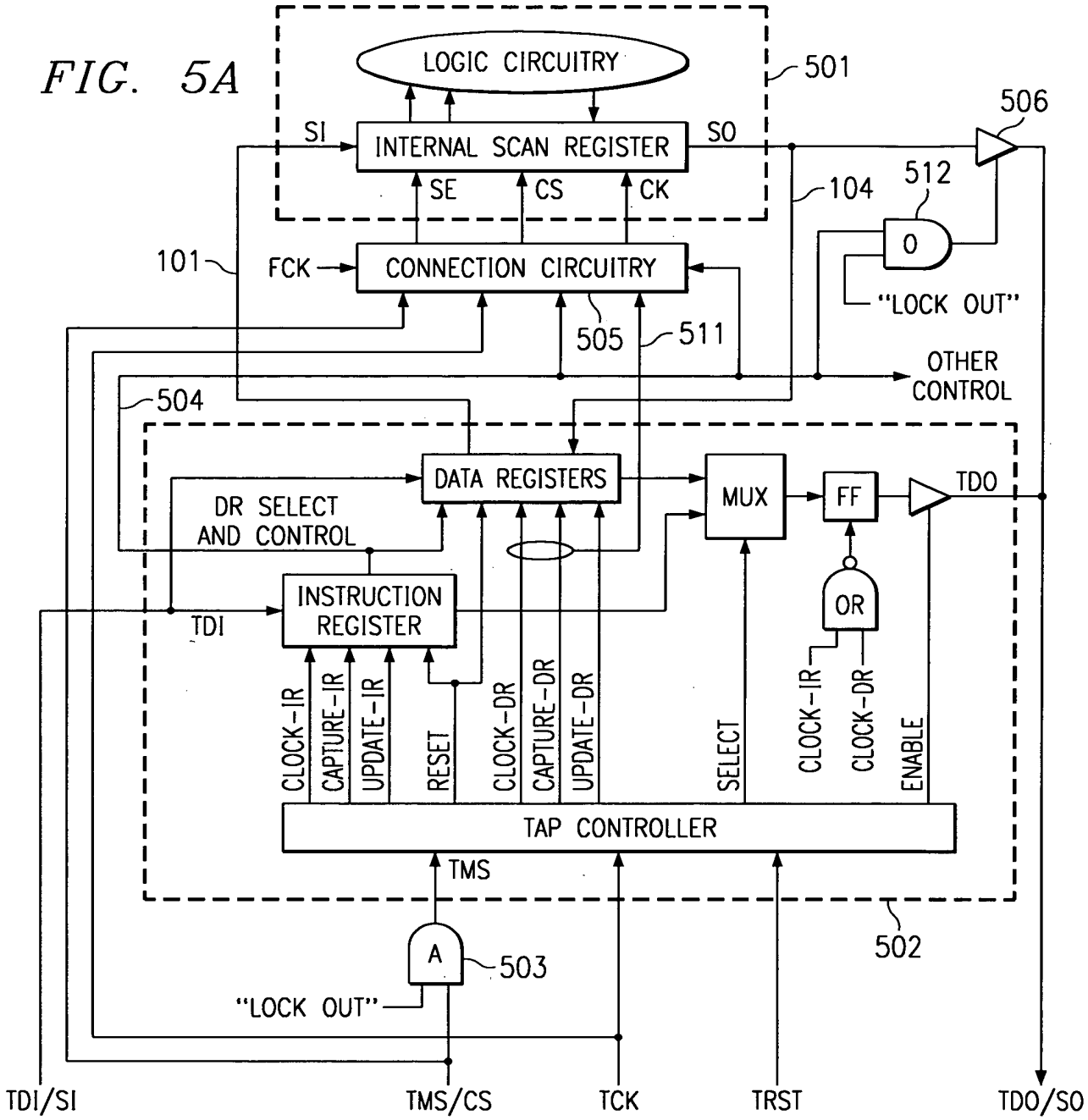


FIG. 4

FIG. 5A



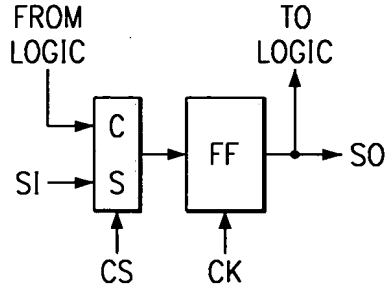


FIG. 5B

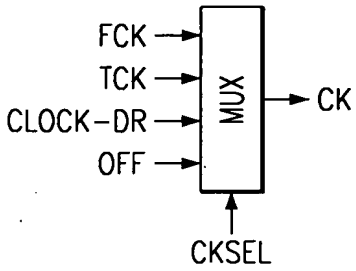


FIG. 5C

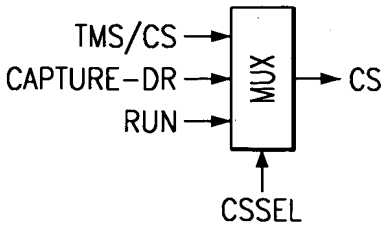


FIG. 5D

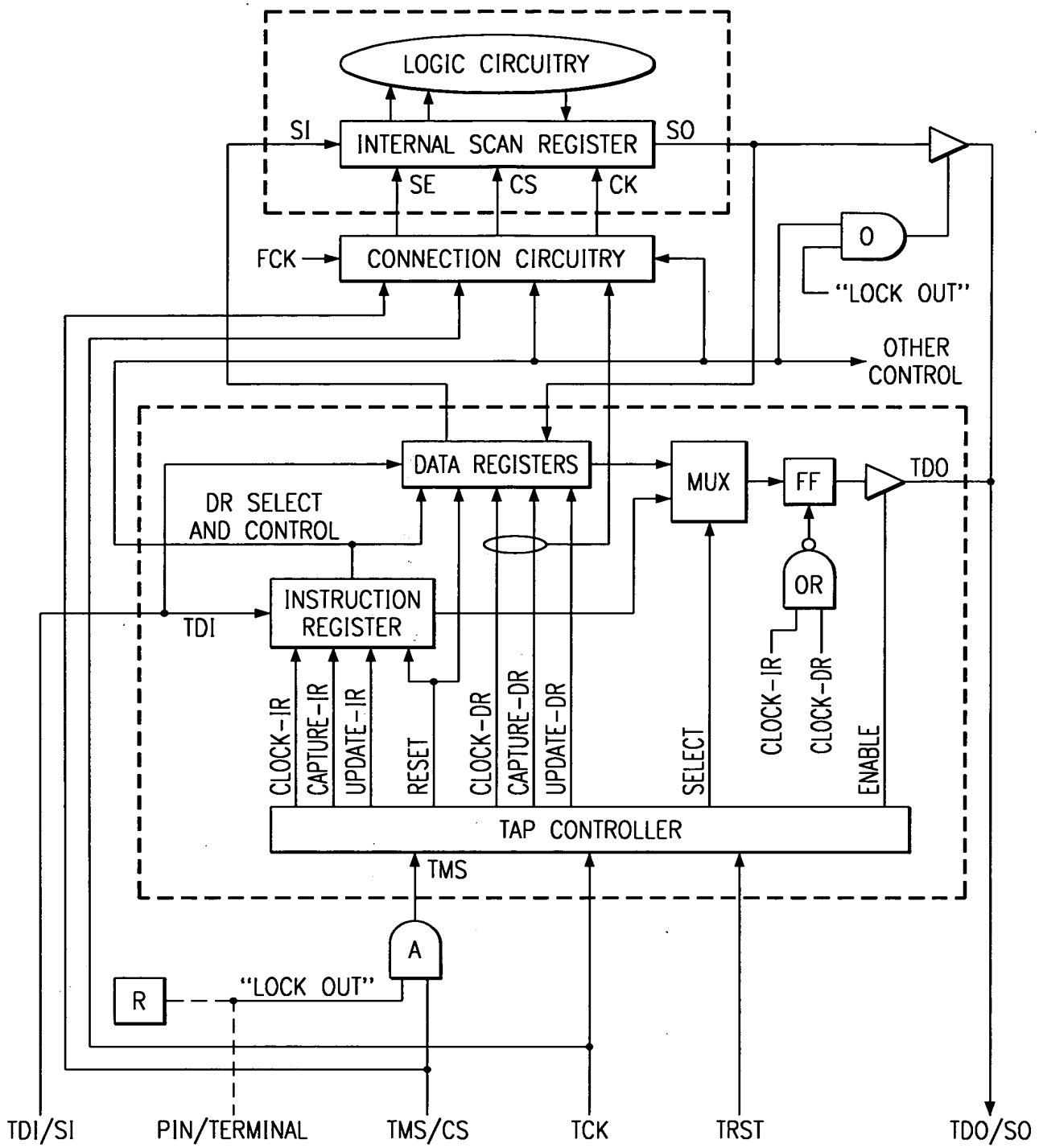

LOGIC CIRCUITRY
SI
INTERNAL SCAN REGISTER
SO
SE
CS
CK
FCK
CONNECTION CIRCUITRY
O
"LOCK OUT"
OTHER CONTROL
DATA REGISTERS
MUX
FF
TDO
DR SELECT AND CONTROL
OR
INSTRUCTION REGISTER
TDI
CLOCK-IR
CAPTURE-IR
UPDATE-IR
RESET
CLOCK-DR
CAPTURE-DR
UPDATE-DR
SELECT
CLOCK-IR
CLOCK-DR
ENABLE
TAP CONTROLLER
TMS
A
R
"LOCK OUT"
TDI/SI
PIN/TERMINAL
TMS/CS
TCK
TRST
TDO/SO

FIG. 6

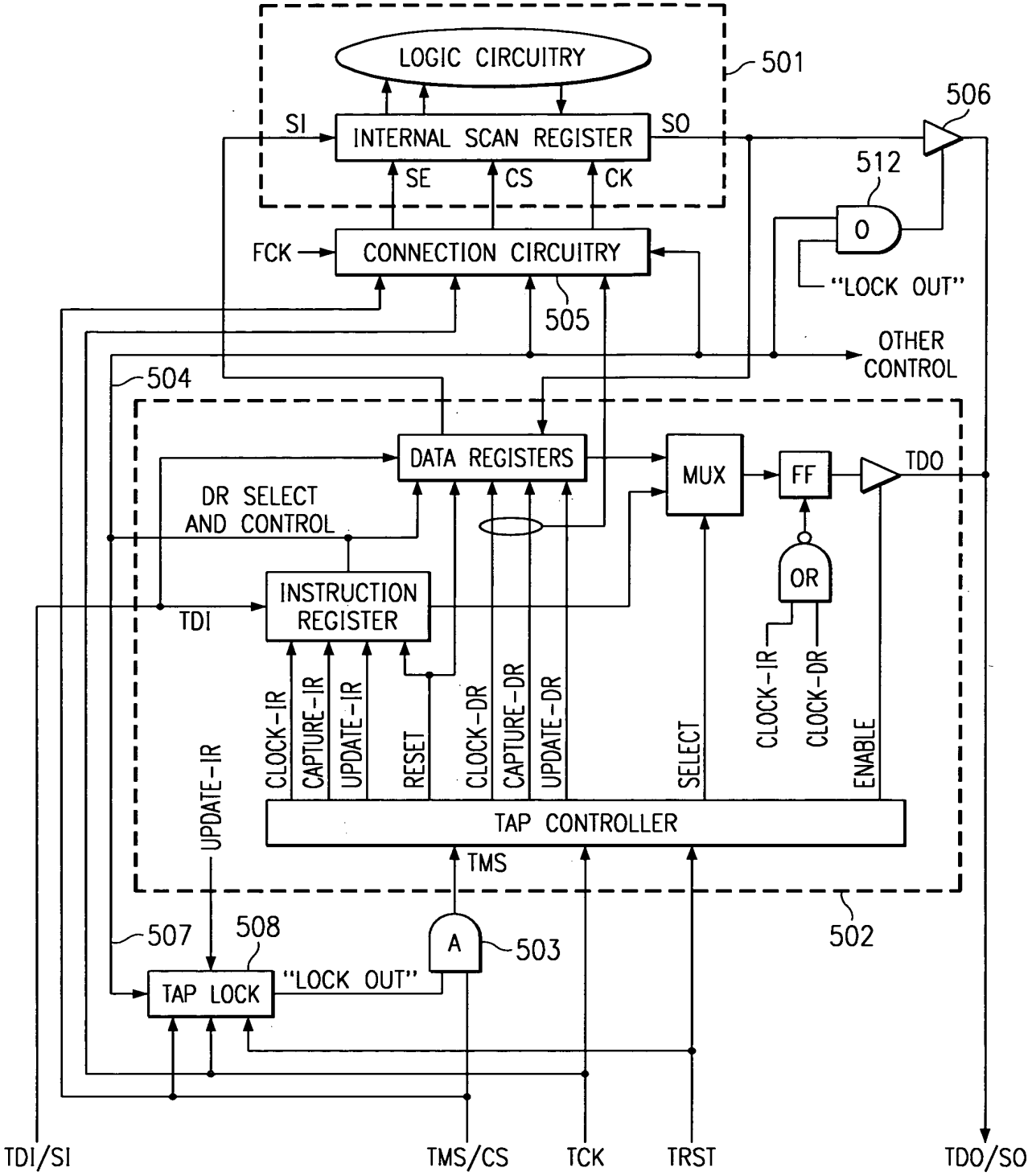

LOGIC CIRCUITRY
501
506
SI
INTERNAL SCAN REGISTER
SO
512
SE
CS
CK
O
FCK
CONNECTION CIRCUITRY
"LOCK OUT"
505
OTHER CONTROL
504
DATA REGISTERS
MUX
FF
TDO
DR SELECT AND CONTROL
OR
INSTRUCTION REGISTER
TDI
CLOCK-IR
CAPTURE-IR
UPDATE-IR
RESET
CLOCK-DR
CAPTURE-DR
UPDATE-DR
SELECT
CLOCK-IR
CLOCK-DR
ENABLE
UPDATE-IR
TAP CONTROLLER
TMS
502
507
508
A
503
TAP LOCK
"LOCK OUT"
TDI/SI
TMS/CS
TCK
TRST
TDO/SO

FIG. 7

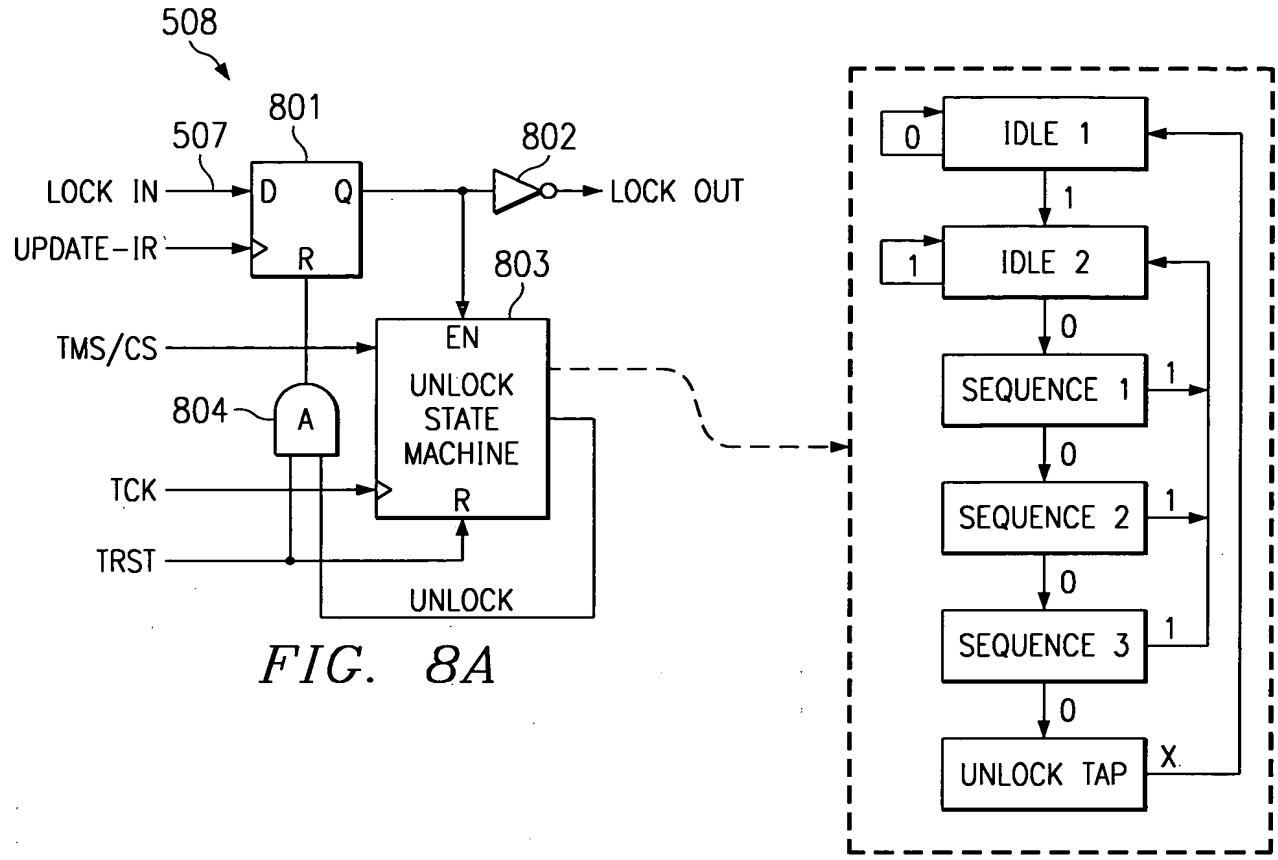


FIG. 8A

FIG. 8B

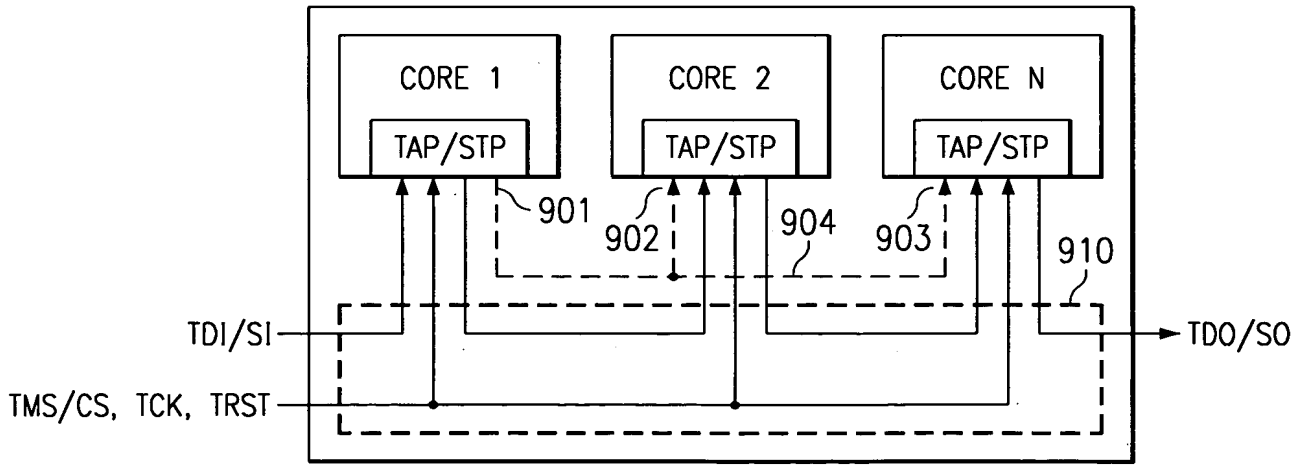
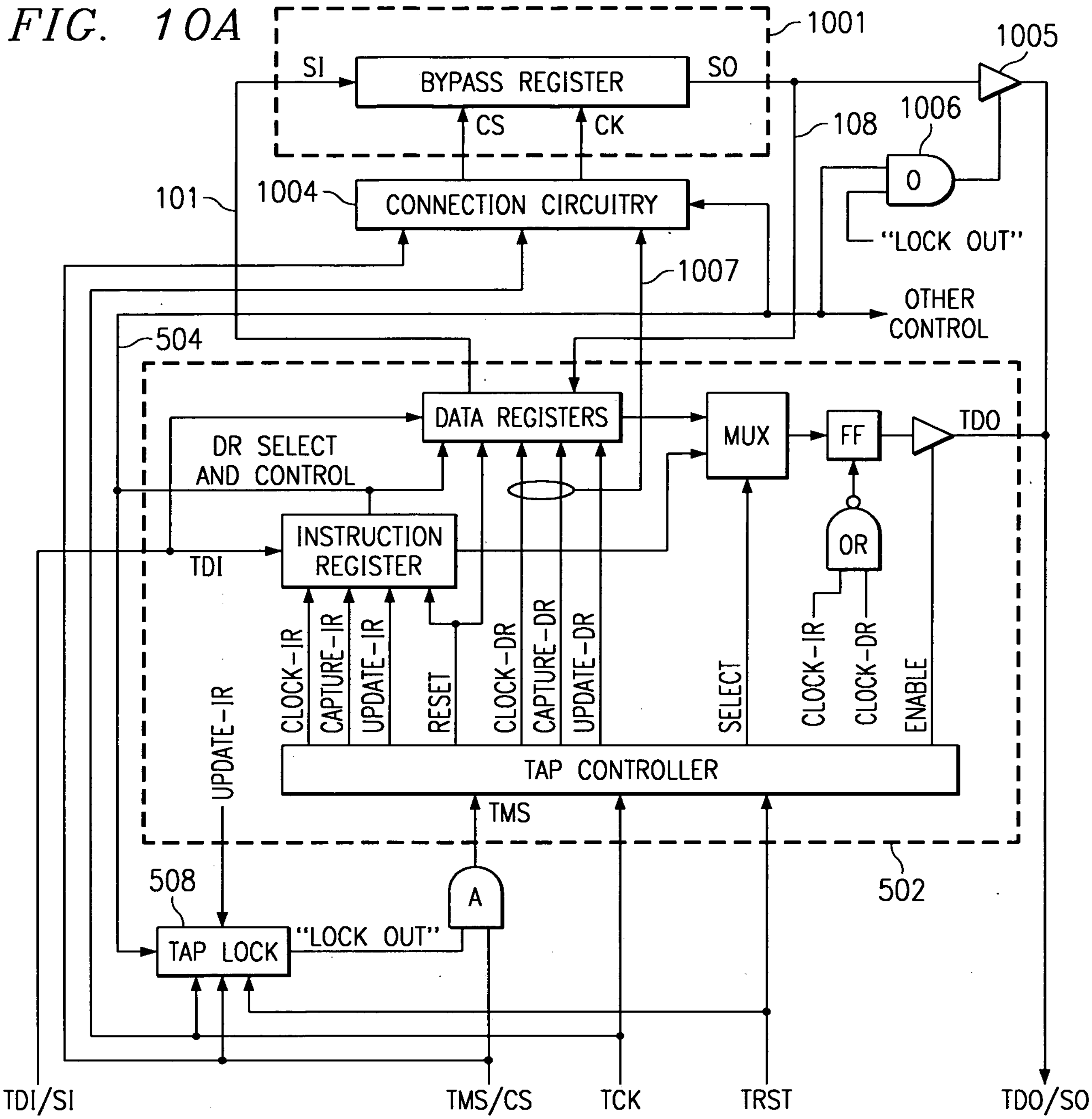


FIG. 9

FIG. 10A



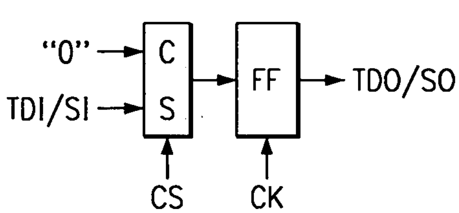


FIG. 10B

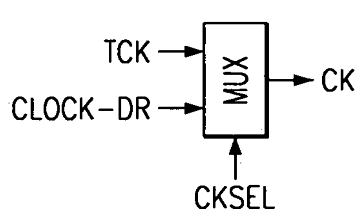


FIG. 10C

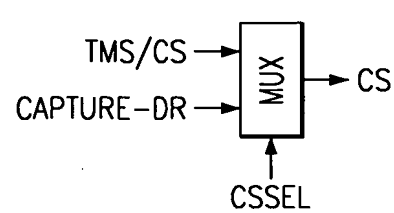


FIG. 10D

FIG. 11

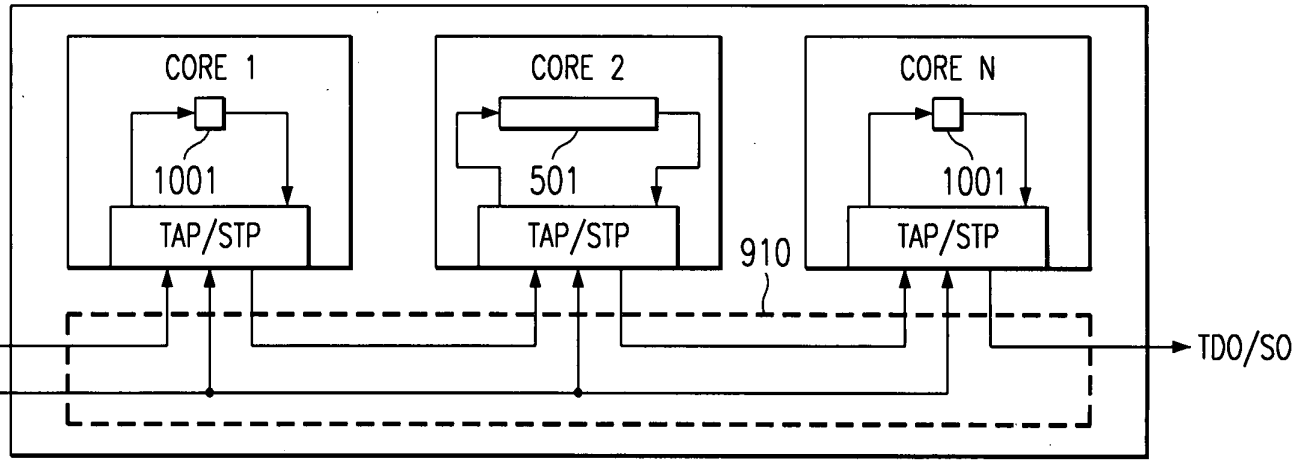

CORE 1
1001
TAP/STP
CORE 2
501
TAP/STP
CORE N
1001
TAP/STP
910
TDI/SI
TMS/CS, TCK, TRST
TDO/SO

FIG. 13

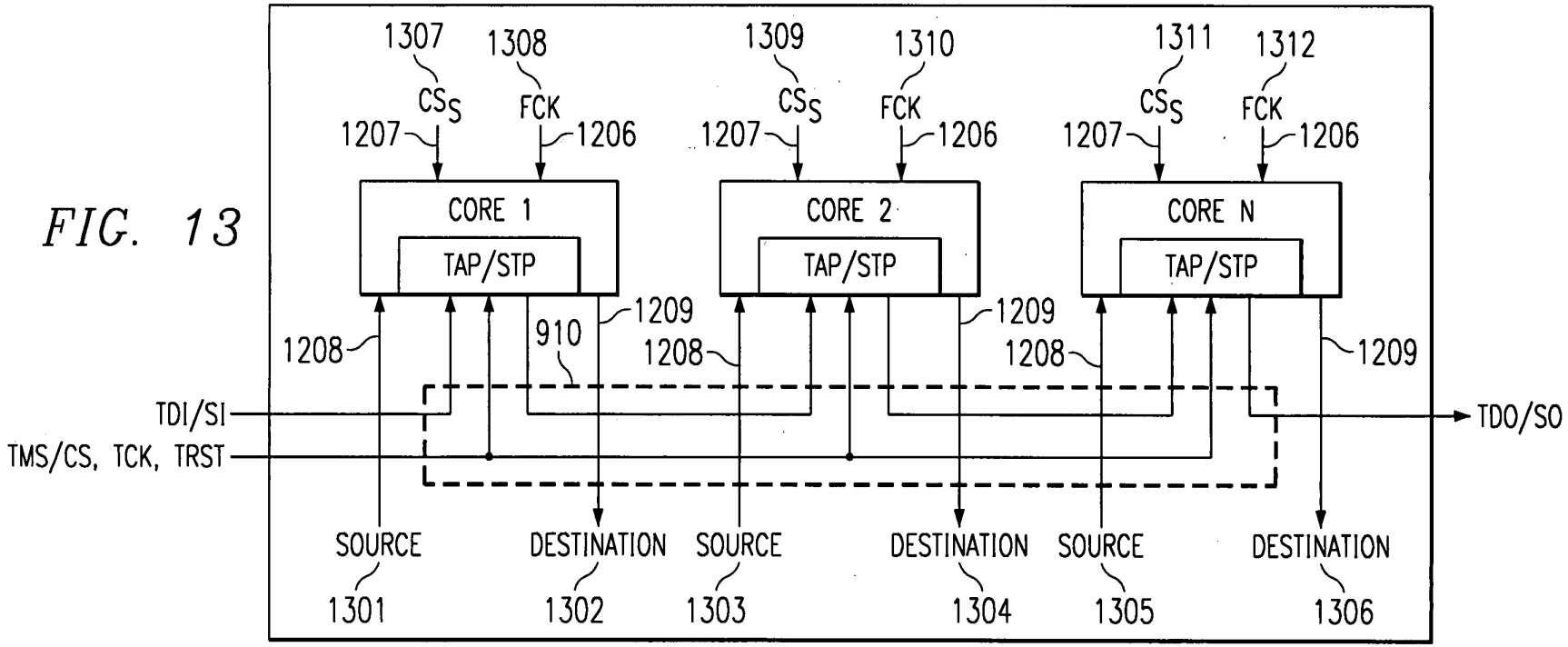
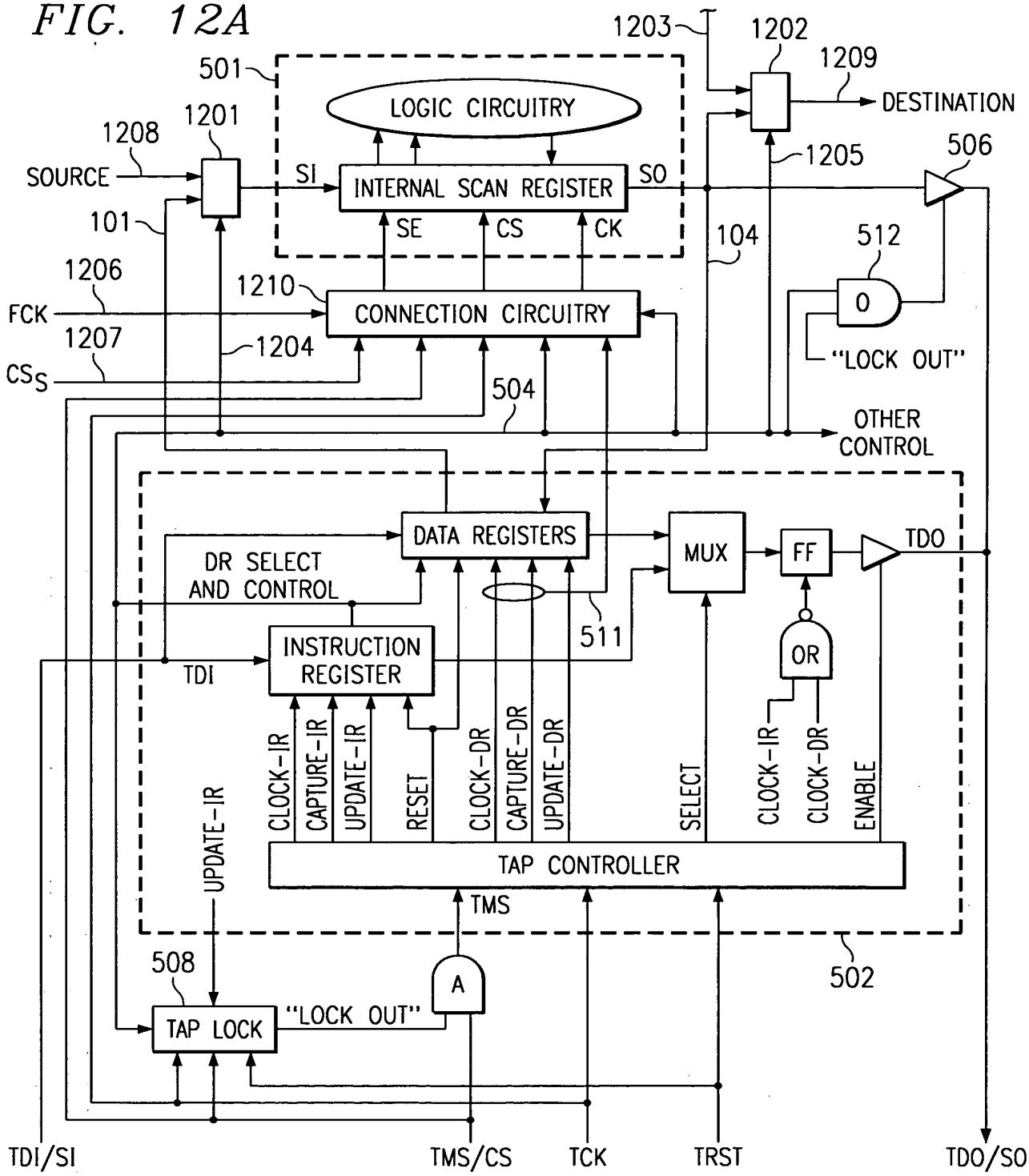

1307
1308
1309
1310
1311
1312
CSS
FCK
1207
1206
CORE 1
TAP/STP
CORE 2
TAP/STP
CORE N
TAP/STP
1208
910
1209
TDI/SI
TMS/CS, TCK, TRST
TDO/SO
SOURCE
DESTINATION
1301
1302
1303
1304
1305
1306

FIG. 12A



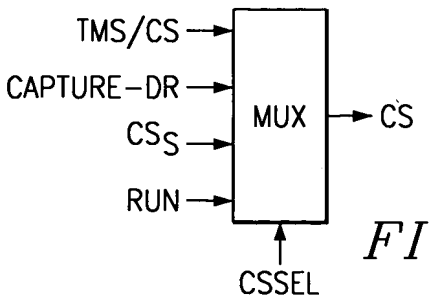
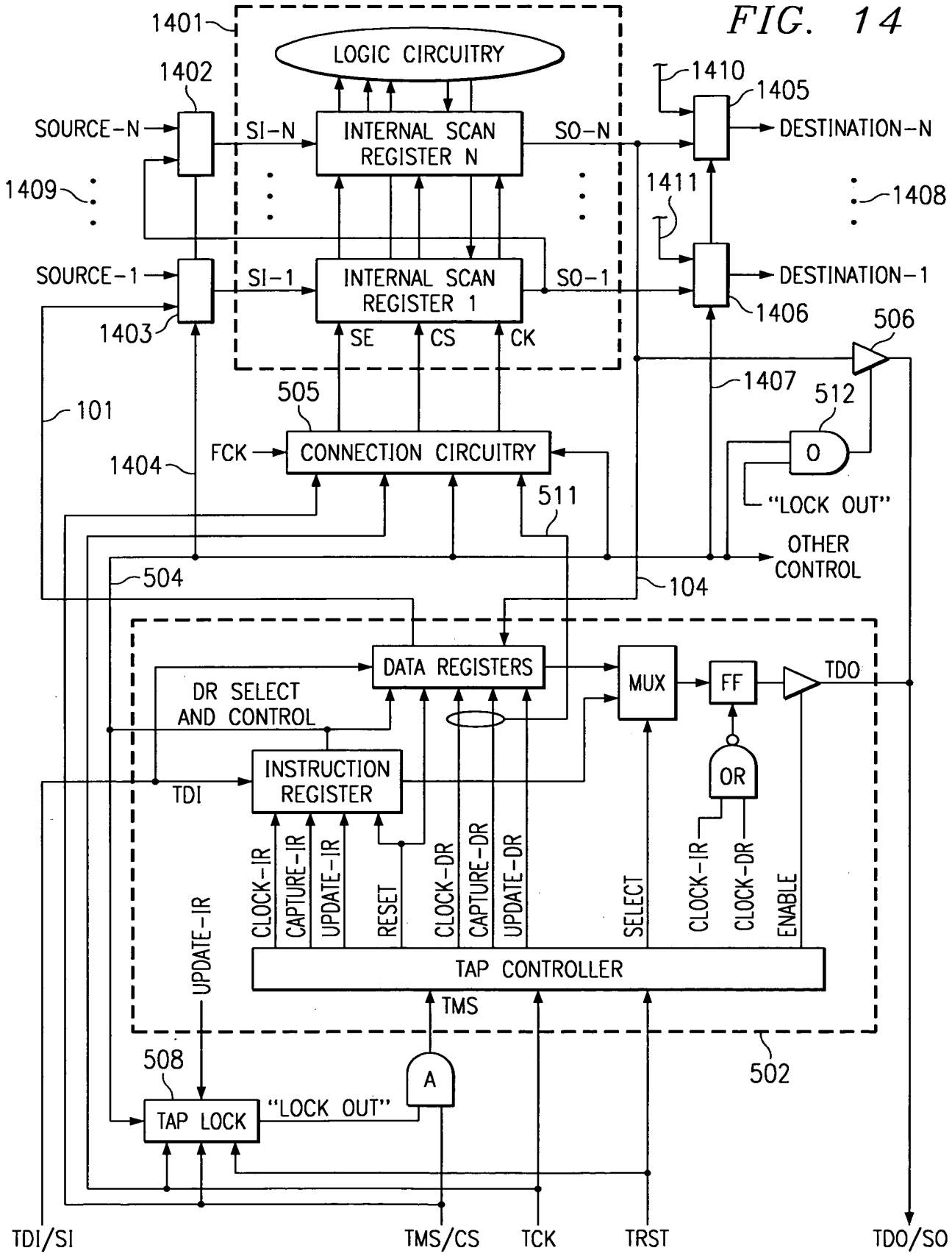


FIG. 12B

FIG. 14


1401
LOGIC CIRCUITRY
1402
SOURCE-N
SI-N
INTERNAL SCAN REGISTER N
SO-N
1410
1405
DESTINATION-N
1409
1411
1408
SOURCE-1
SI-1
INTERNAL SCAN REGISTER 1
SO-1
DESTINATION-1
1403
1406
SE
CS
CK
506
1407
505
512
101
FCK
CONNECTION CIRCUITRY
1404
"LOCK OUT"
511
OTHER CONTROL
504
104
DATA REGISTERS
MUX
FF
TDO
DR SELECT AND CONTROL
INSTRUCTION REGISTER
OR
TDI
CLOCK-IR
CAPTURE-IR
UPDATE-IR
RESET
CLOCK-DR
CAPTURE-DR
UPDATE-DR
SELECT
CLOCK-IR
CLOCK-DR
ENABLE
UPDATE-IR
TAP CONTROLLER
TMS
502
508
A
TAP LOCK
"LOCK OUT"
TDI/SI
TMS/CS
TCK
TRST
TDO/SO

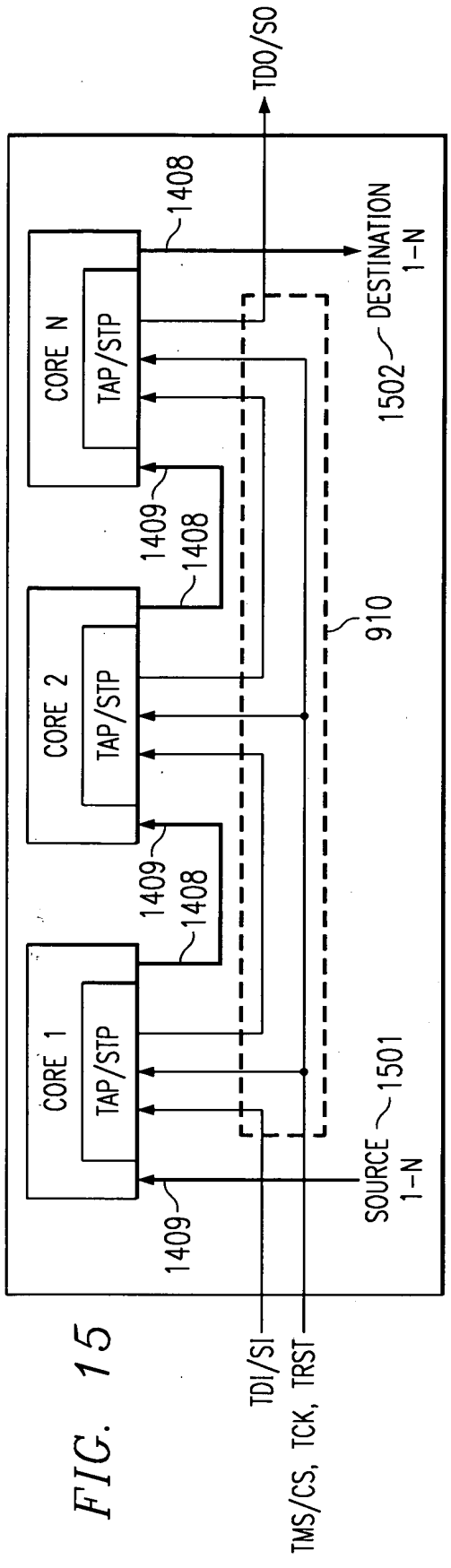

TDO/SO
CORE 1
TAP/STP
CORE 2
TAP/STP
CORE N
TAP/STP
1408
1409
1408
1409
1408
1409
910
1502
DESTINATION
1-N
SOURCE
1-N
1501
1409
TDI/SI
TMS/CS, TCK, TRST

FIG. 15

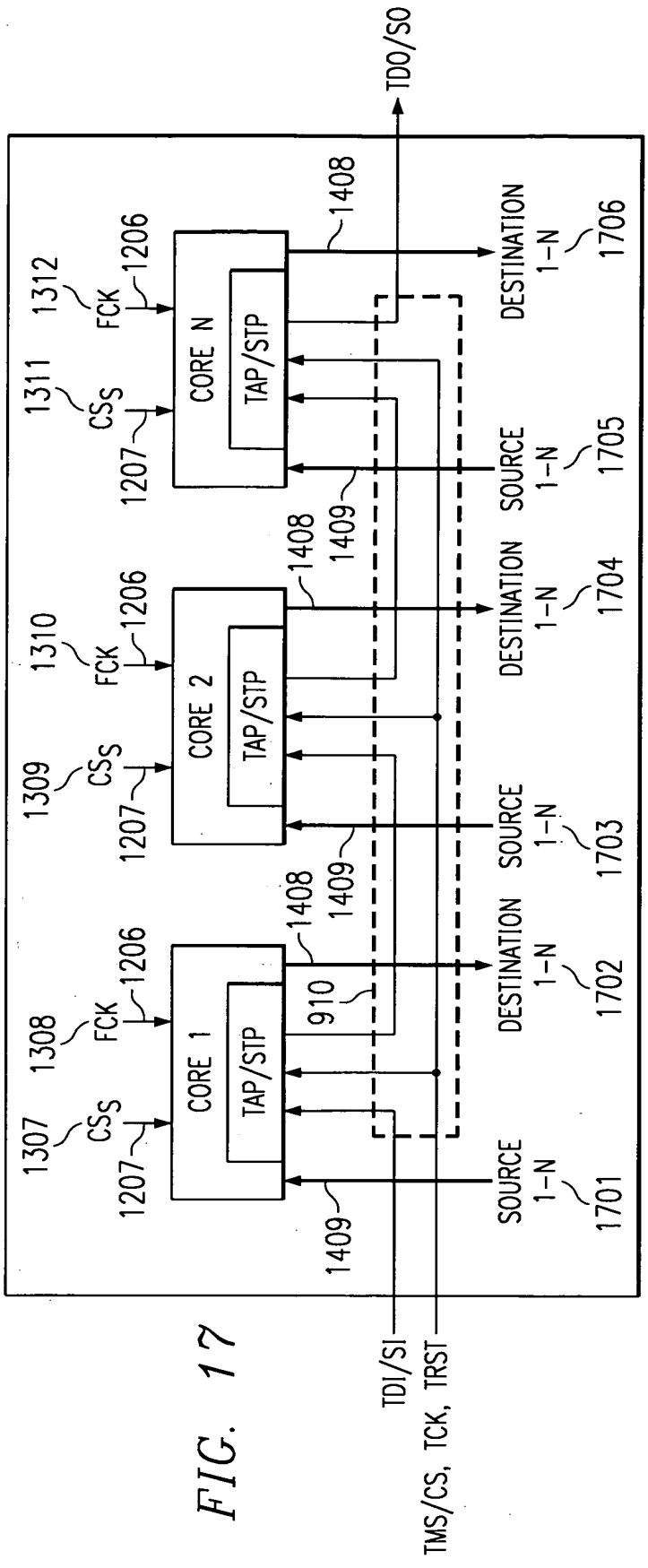
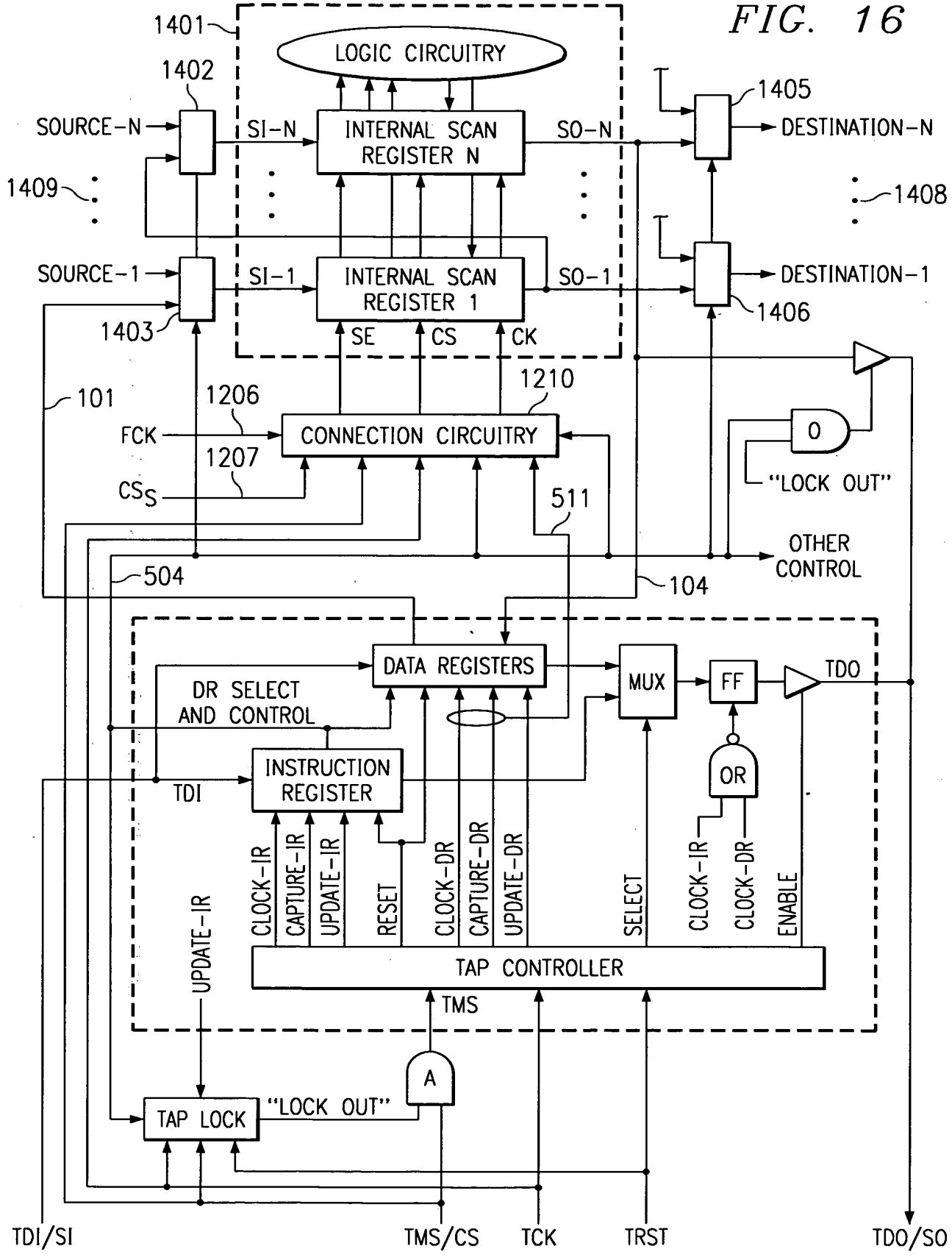

TDO/SO
1307
1308
FCK
1206
CSS
1207
CORE 1
TAP/STP
1309
1310
FCK
1206
CSS
1207
CORE 2
TAP/STP
1311
1312
FCK
1206
CSS
1207
CORE N
TAP/STP
1408
1409
910
DESTINATION
1-N
1702
1703
1704
1706
SOURCE
1-N
1701
1705
1409
TDI/SI
TMS/CS, TCK, TRST

FIG. 17

FIG. 16


1401
LOGIC CIRCUITRY
1402
SOURCE-N
SI-N
INTERNAL SCAN REGISTER N
SO-N
1405
DESTINATION-N
1409
1408
SOURCE-1
SI-1
INTERNAL SCAN REGISTER 1
SO-1
DESTINATION-1
1406
1403
SE
CS
CK
1210
101
1206
FCK
CONNECTION CIRCUITRY
1207
CSS
511
0
"LOCK OUT"
OTHER CONTROL
504
104
DATA REGISTERS
MUX
FF
TDO
DR SELECT AND CONTROL
INSTRUCTION REGISTER
TDI
OR
CLOCK-IR
CAPTURE-IR
UPDATE-IR
RESET
CLOCK-DR
CAPTURE-DR
UPDATE-DR
SELECT
CLOCK-IR
CLOCK-DR
ENABLE
UPDATE-IR
TAP CONTROLLER
TMS
A
TAP LOCK
"LOCK OUT"
TDI/SI
TMS/CS
TCK
TRST
TDO/SO

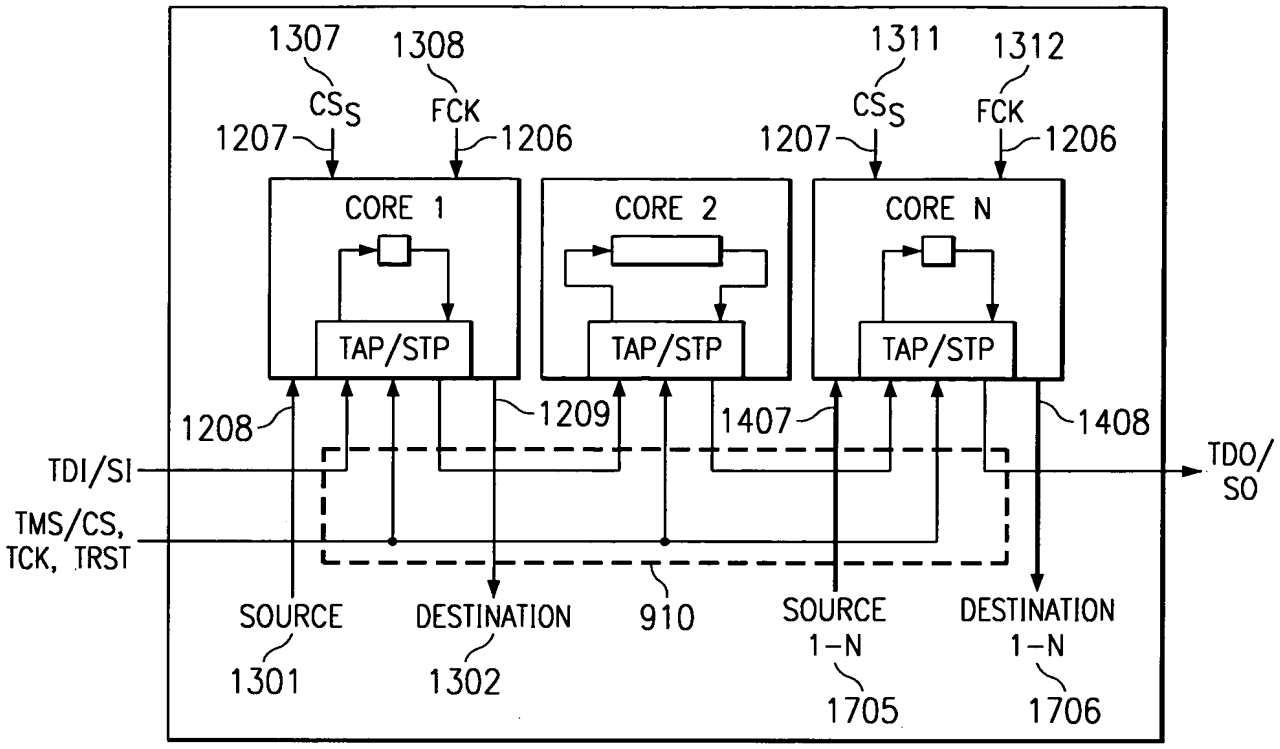


FIG. 18

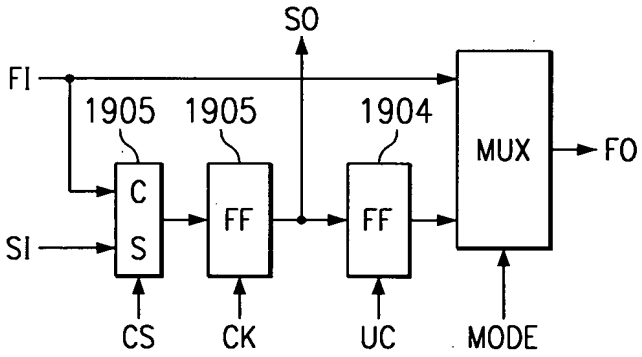


FIG. 19B

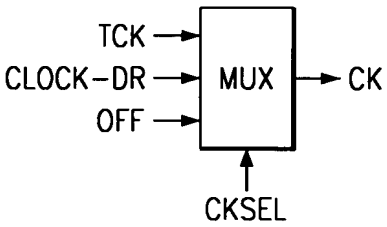


FIG. 19C

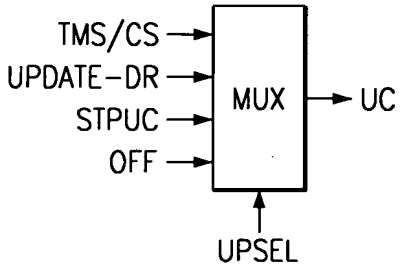


FIG. 19D

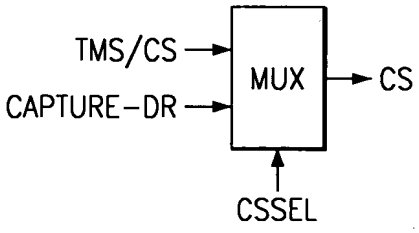


FIG. 19E

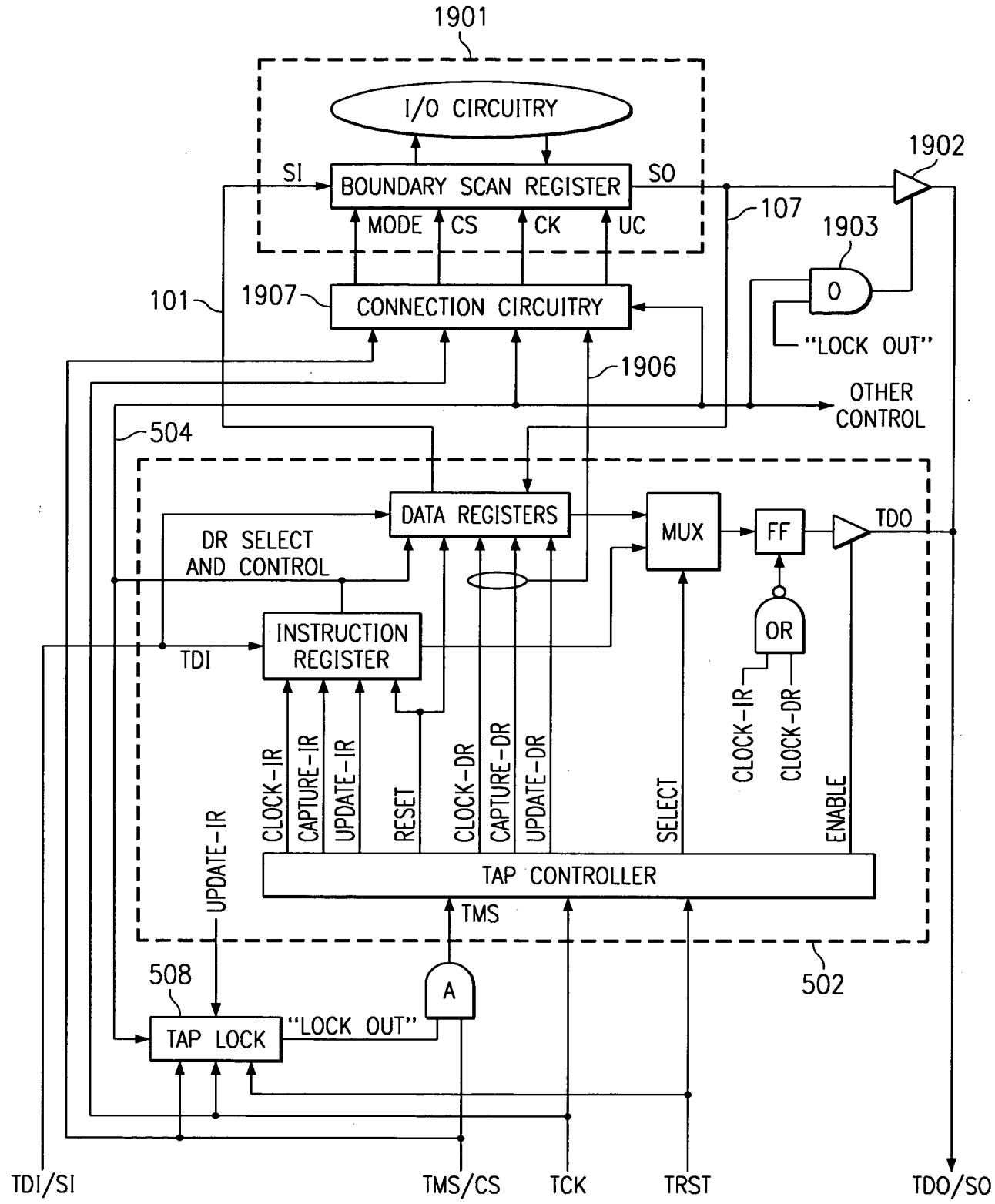

1901
I/O CIRCUITRY
SI
BOUNDARY SCAN REGISTER
SO
MODE
CS
CK
UC
1902
107
1903
0
"LOCK OUT"
101
1907
CONNECTION CIRCUITRY
1906
OTHER CONTROL
504
DATA REGISTERS
MUX
FF
TDO
DR SELECT AND CONTROL
OR
INSTRUCTION REGISTER
TDI
CLOCK-IR
CAPTURE-IR
UPDATE-IR
RESET
CLOCK-DR
CAPTURE-DR
UPDATE-DR
SELECT
CLOCK-IR
CLOCK-DR
ENABLE
UPDATE-IR
TAP CONTROLLER
TMS
502
508
A
TAP LOCK
"LOCK OUT"
TDI/SI
TMS/CS
TCK
TRST
TDO/SO

FIG. 19A

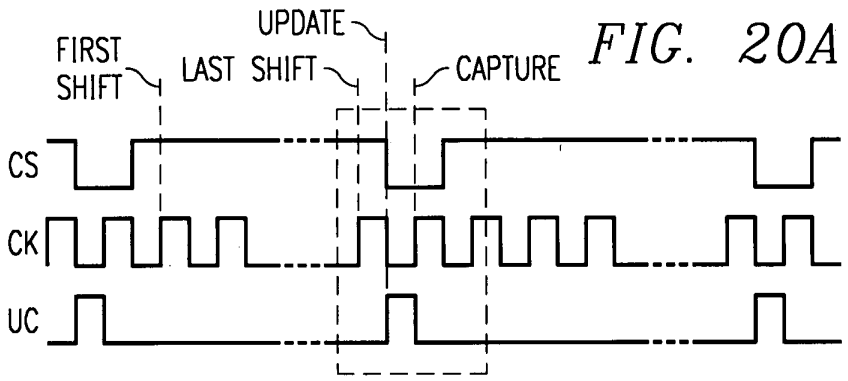


FIG. 20A

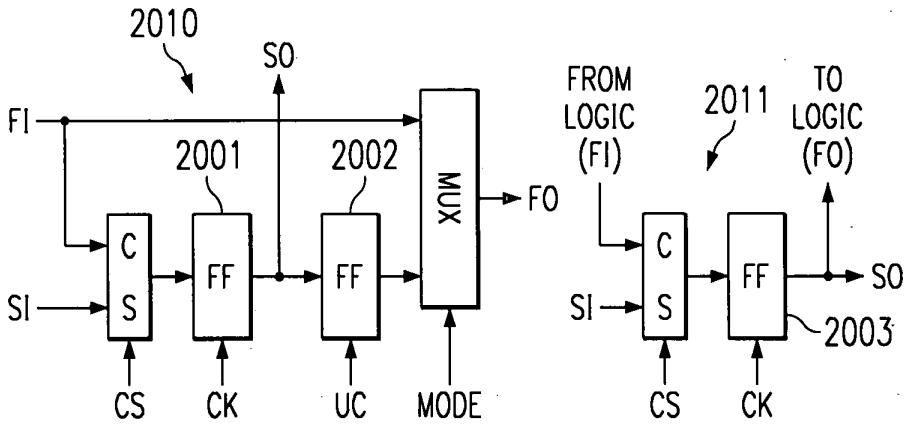


FIG. 20C

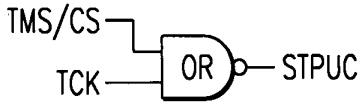


FIG. 20B

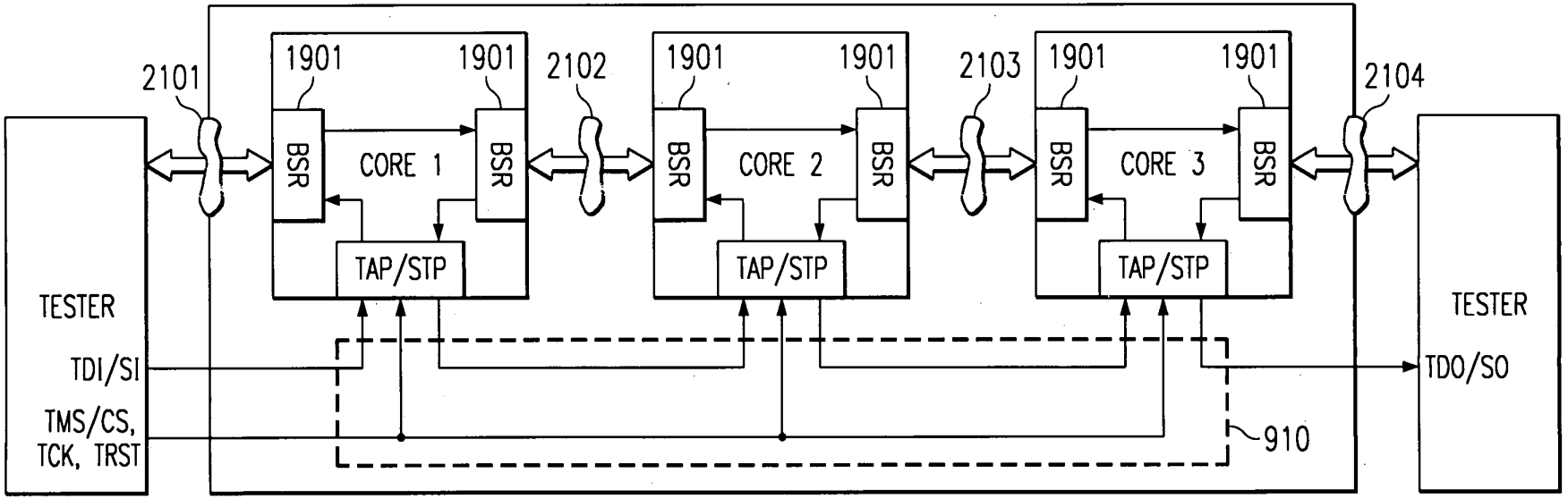


FIG. 21

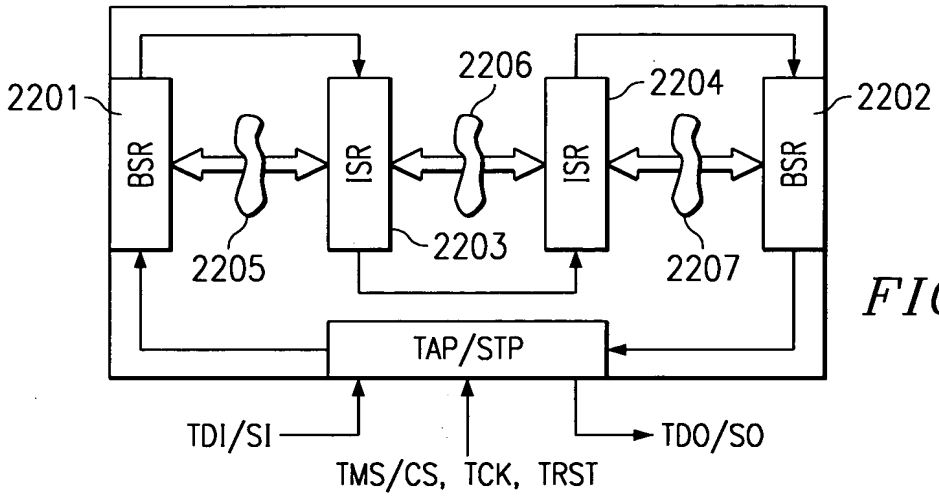
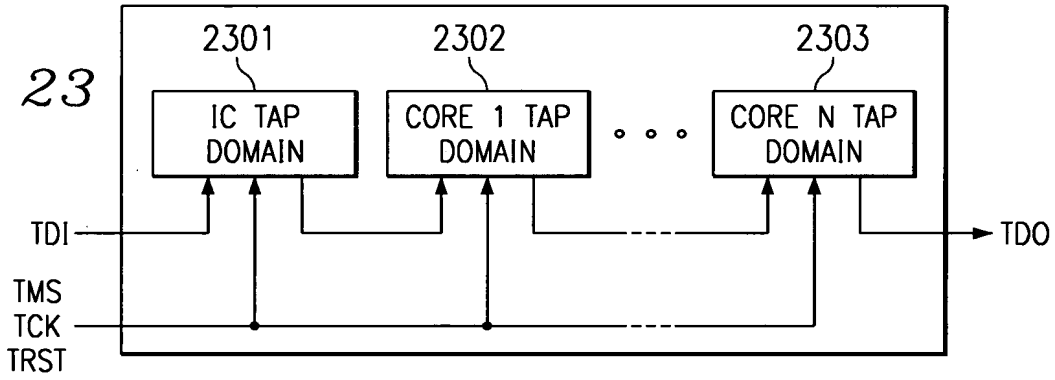


FIG. 22

FIG. 23



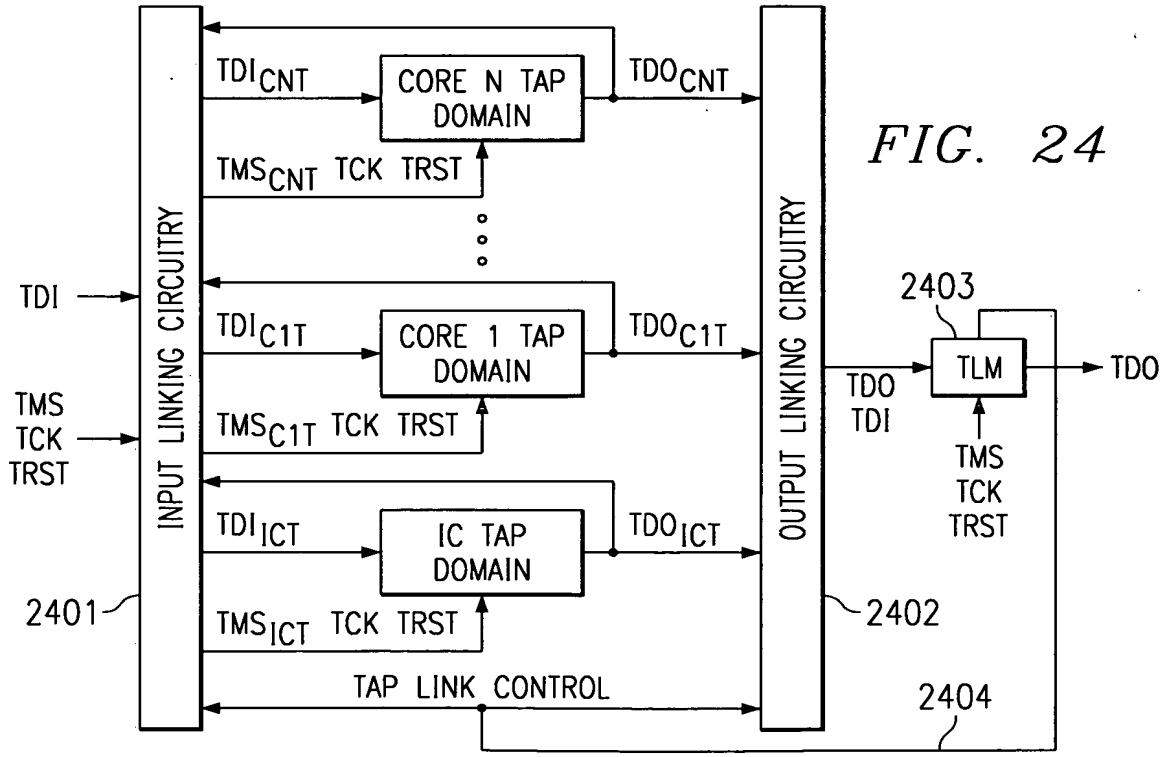


FIG. 24

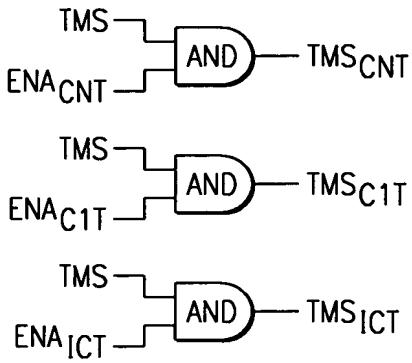


FIG. 25

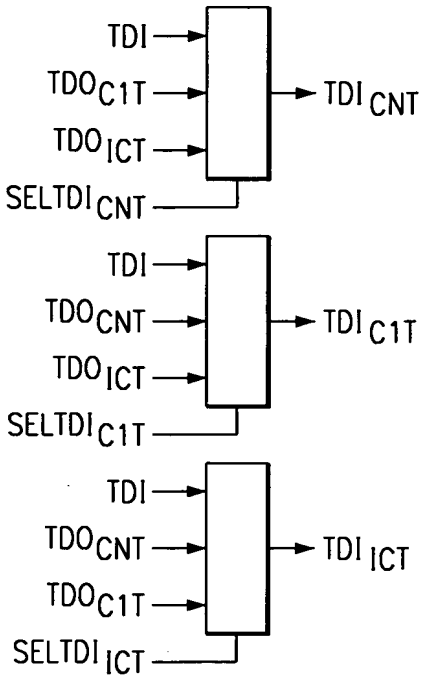


FIG. 26

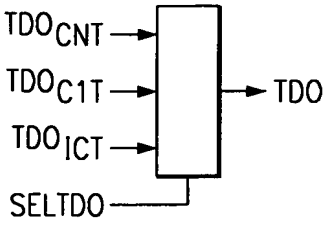


FIG. 27

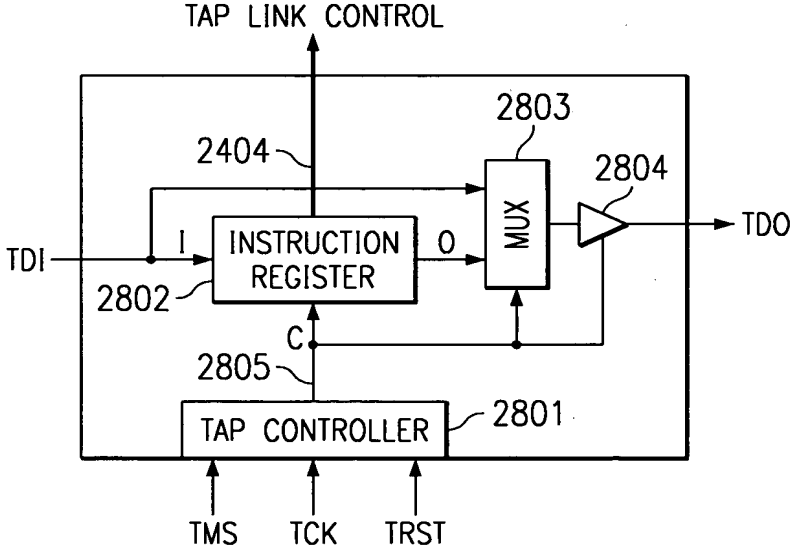


FIG. 28A

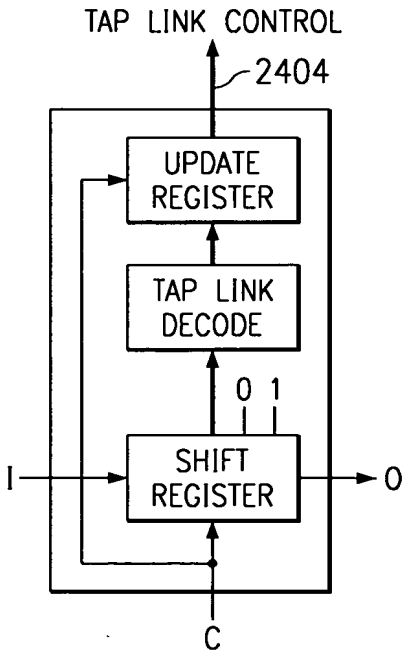


FIG. 28B

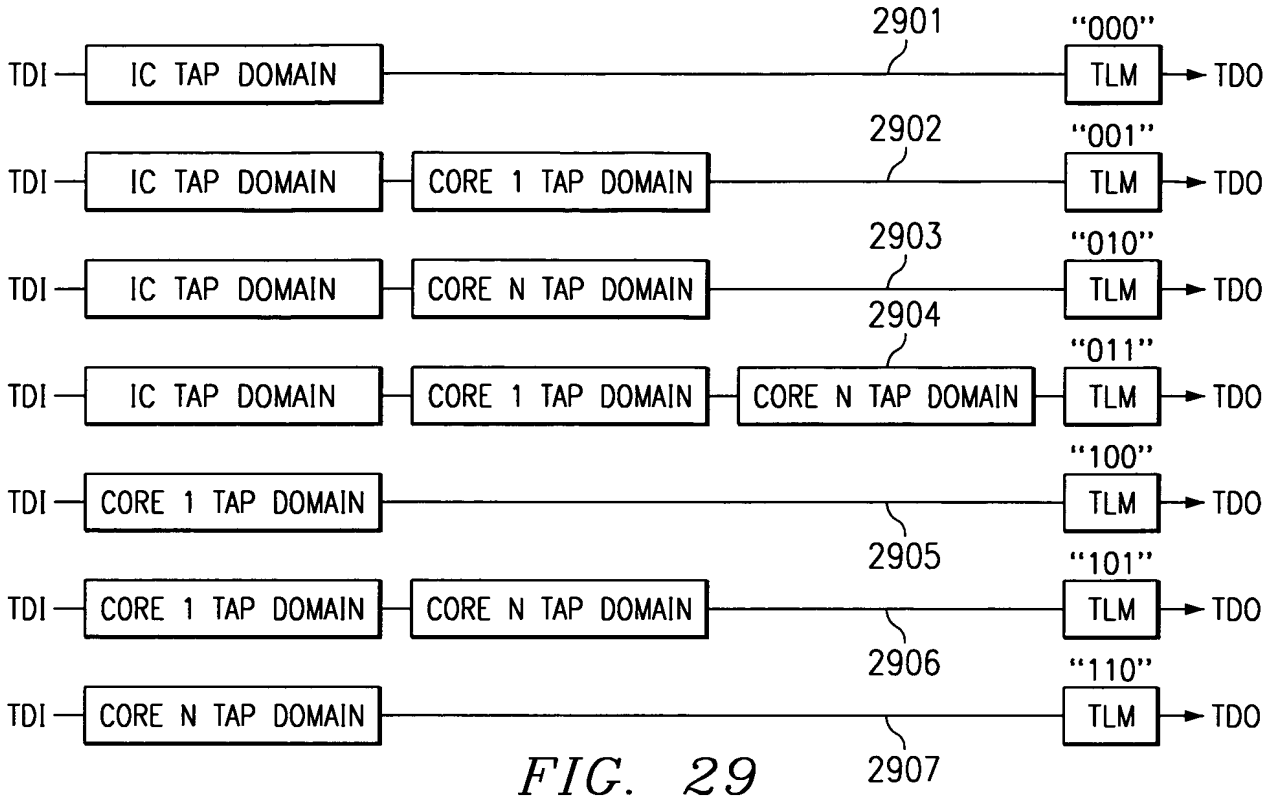

2901
"000"
TDI
IC TAP DOMAIN
TLM
TDO
2902
"001"
TDI
IC TAP DOMAIN
CORE 1 TAP DOMAIN
TLM
TDO
2903
"010"
TDI
IC TAP DOMAIN
CORE N TAP DOMAIN
TLM
TDO
2904
"011"
TDI
IC TAP DOMAIN
CORE 1 TAP DOMAIN
CORE N TAP DOMAIN
TLM
TDO
"100"
TDI
CORE 1 TAP DOMAIN
TLM
TDO
2905
"101"
TDI
CORE 1 TAP DOMAIN
CORE N TAP DOMAIN
TLM
TDO
2906
"110"
TDI
CORE N TAP DOMAIN
TLM
TDO
2907

FIG. 29

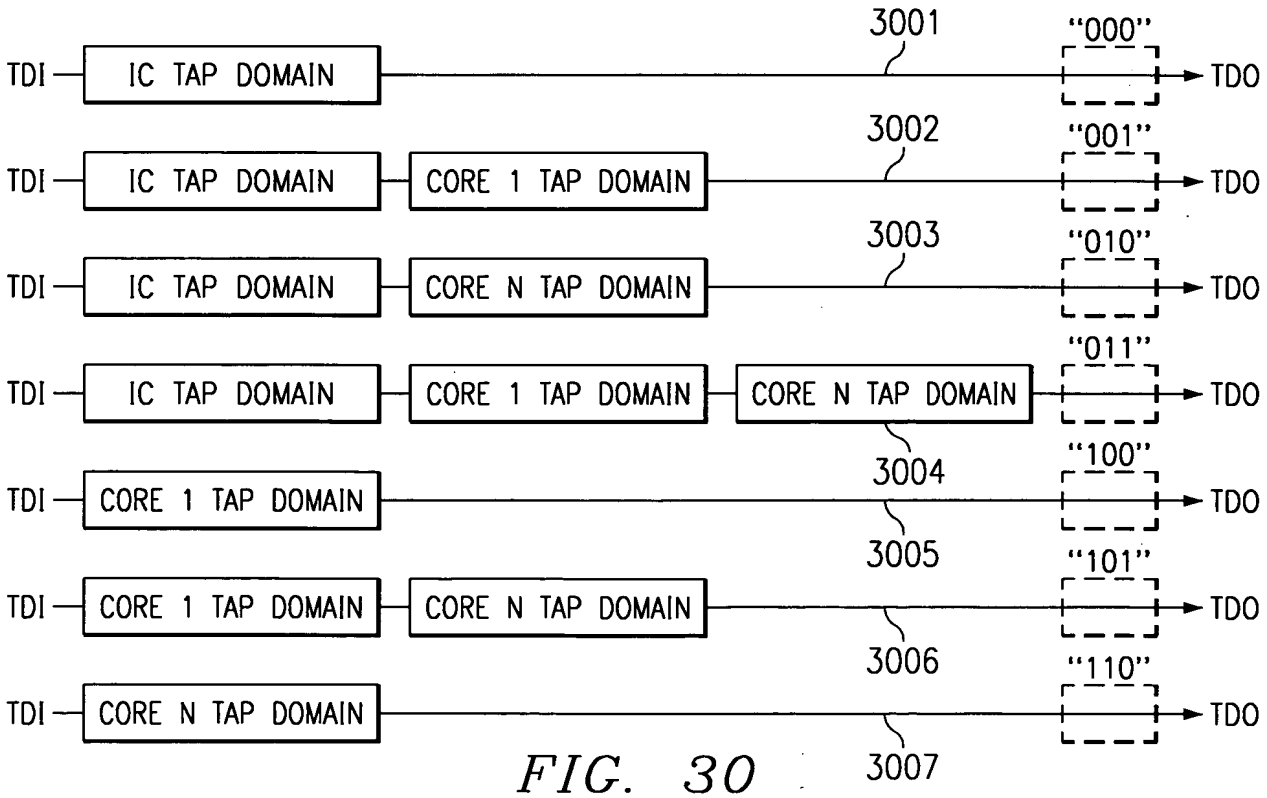

3001
"000"
TDI
IC TAP DOMAIN
TDO
3002
"001"
TDI
IC TAP DOMAIN
CORE 1 TAP DOMAIN
TDO
3003
"010"
TDI
IC TAP DOMAIN
CORE N TAP DOMAIN
TDO
"011"
TDI
IC TAP DOMAIN
CORE 1 TAP DOMAIN
CORE N TAP DOMAIN
TDO
3004
"100"
TDI
CORE 1 TAP DOMAIN
TDO
3005
"101"
TDI
CORE 1 TAP DOMAIN
CORE N TAP DOMAIN
TDO
3006
"110"
TDI
CORE N TAP DOMAIN
TDO
3007

FIG. 30

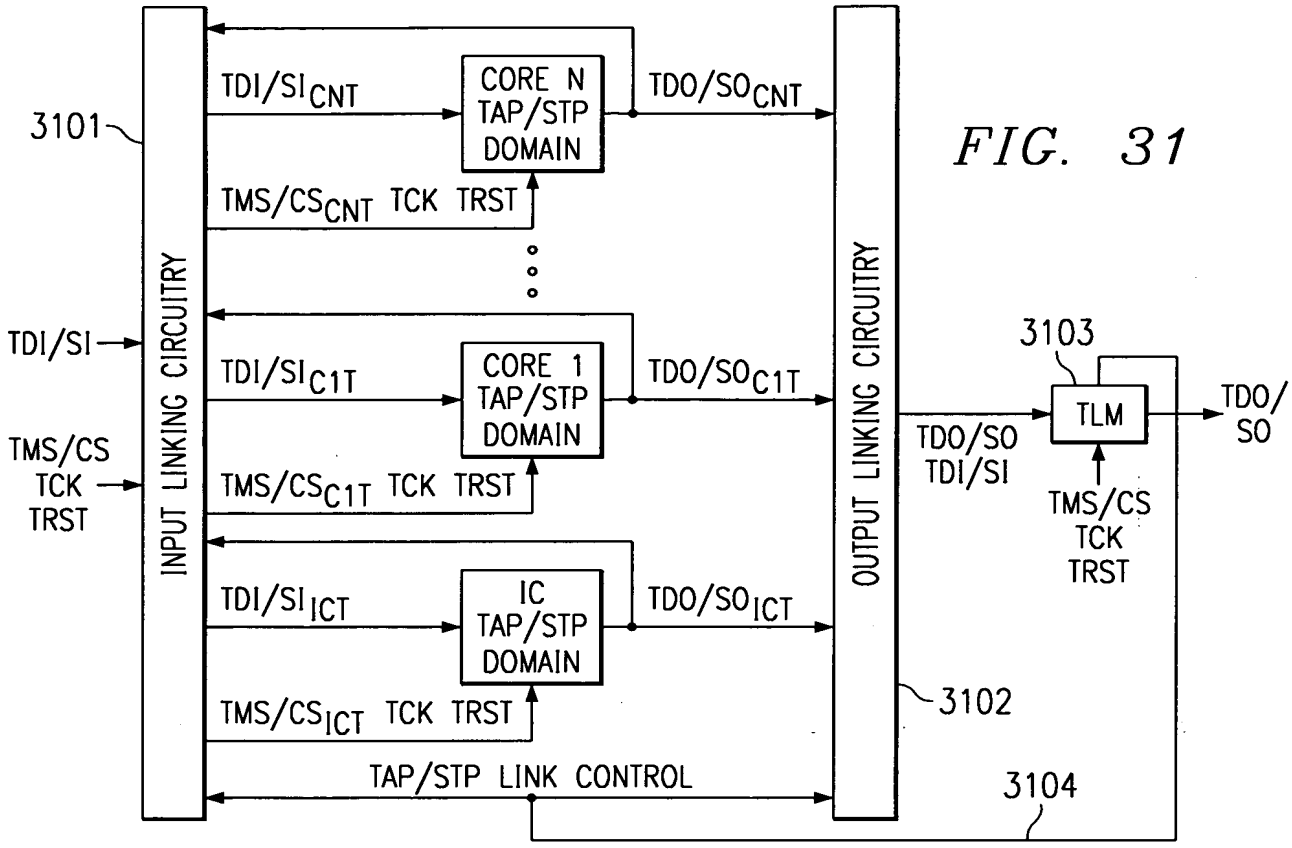


FIG. 31

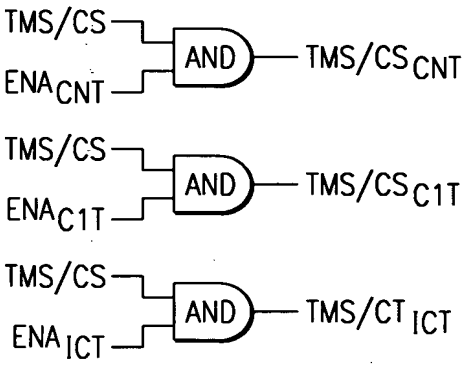


FIG. 32

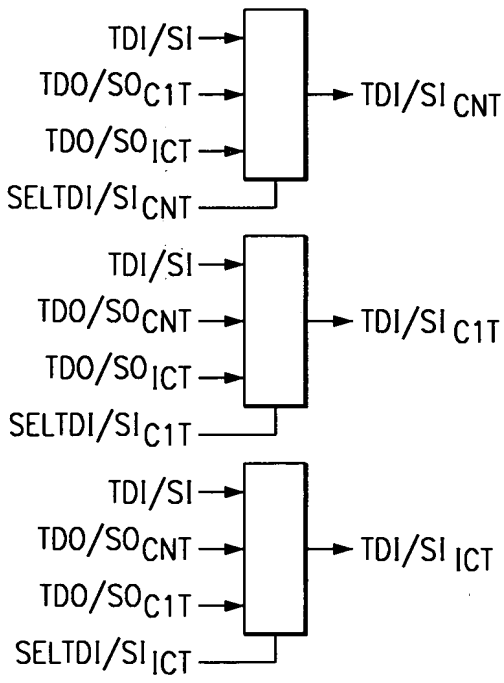


FIG. 33

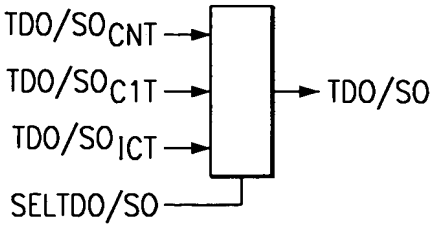


FIG. 34

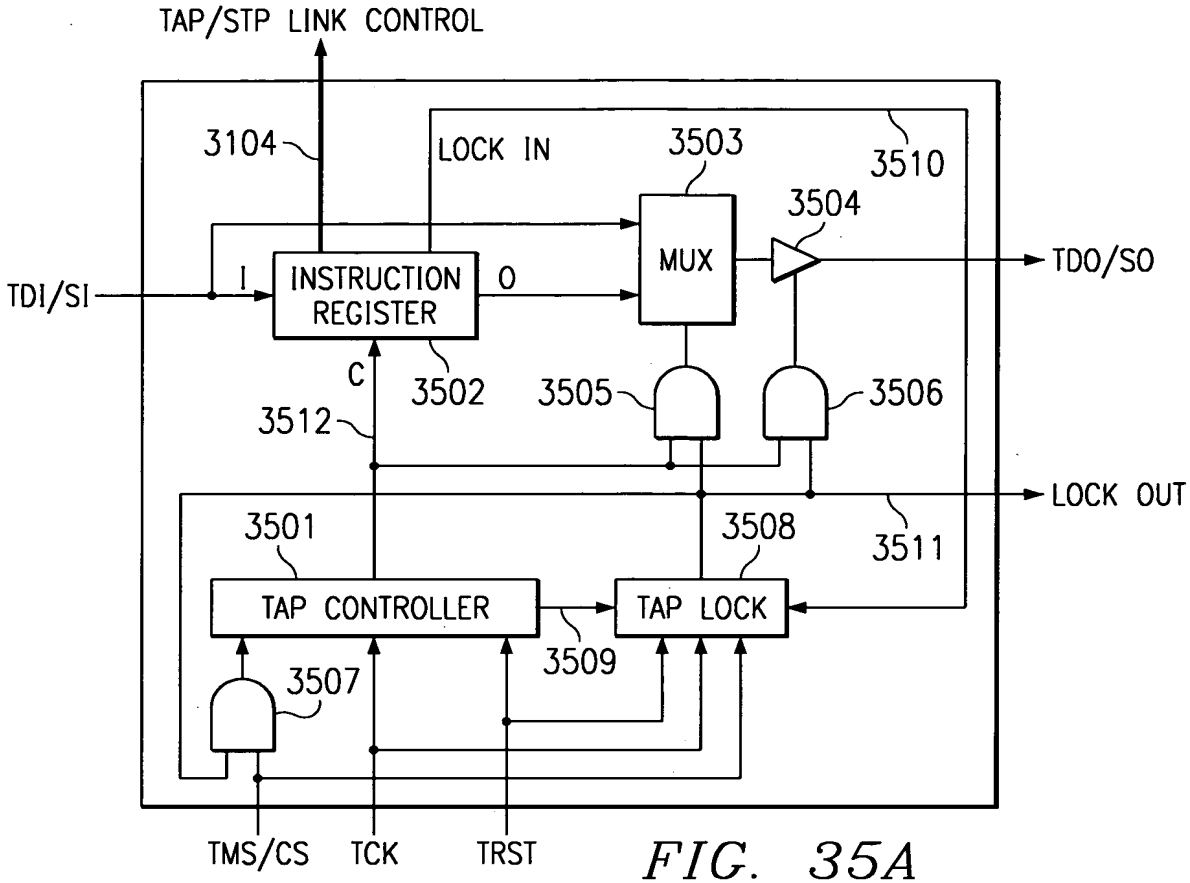


FIG. 35A

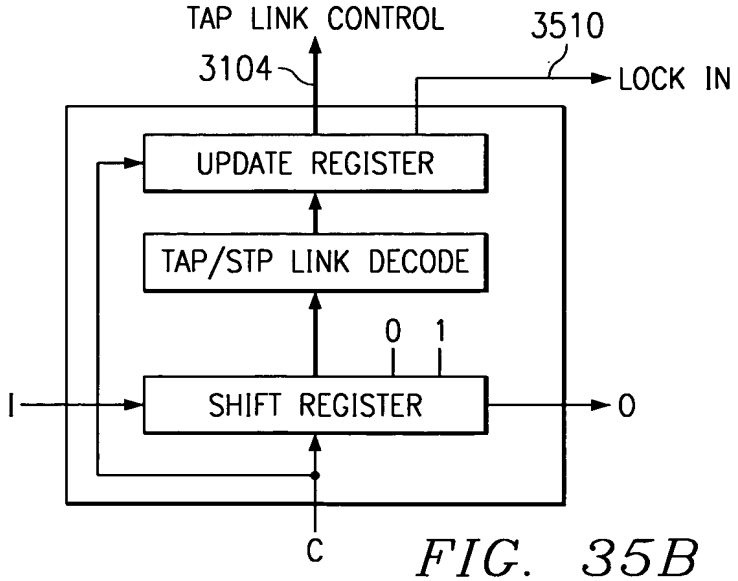


FIG. 35B

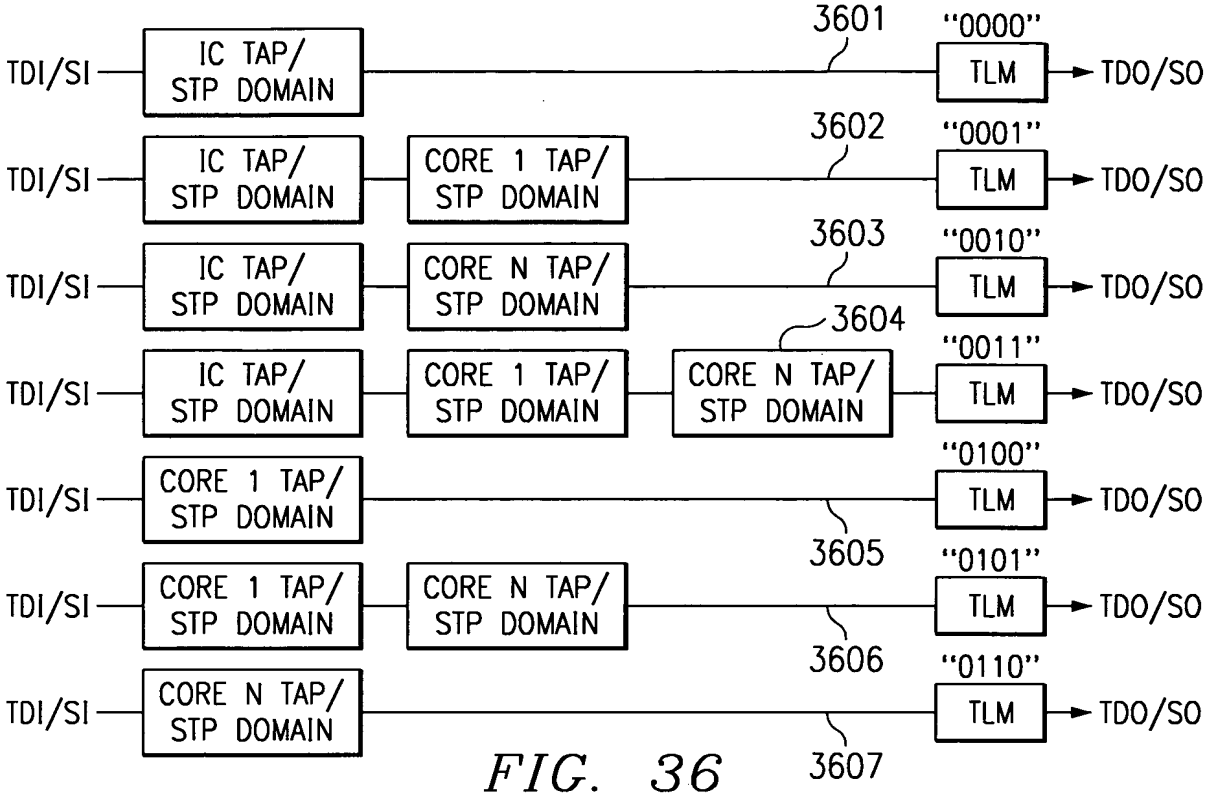

3601
"0000"
TDI/SI
IC TAP/ STP DOMAIN
TLM
TDO/SO
3602
"0001"
CORE 1 TAP/ STP DOMAIN
3603
"0010"
CORE N TAP/ STP DOMAIN
3604
"0011"
CORE N TAP/ STP DOMAIN
"0100"
3605
"0101"
3606
"0110"
3607

FIG. 36

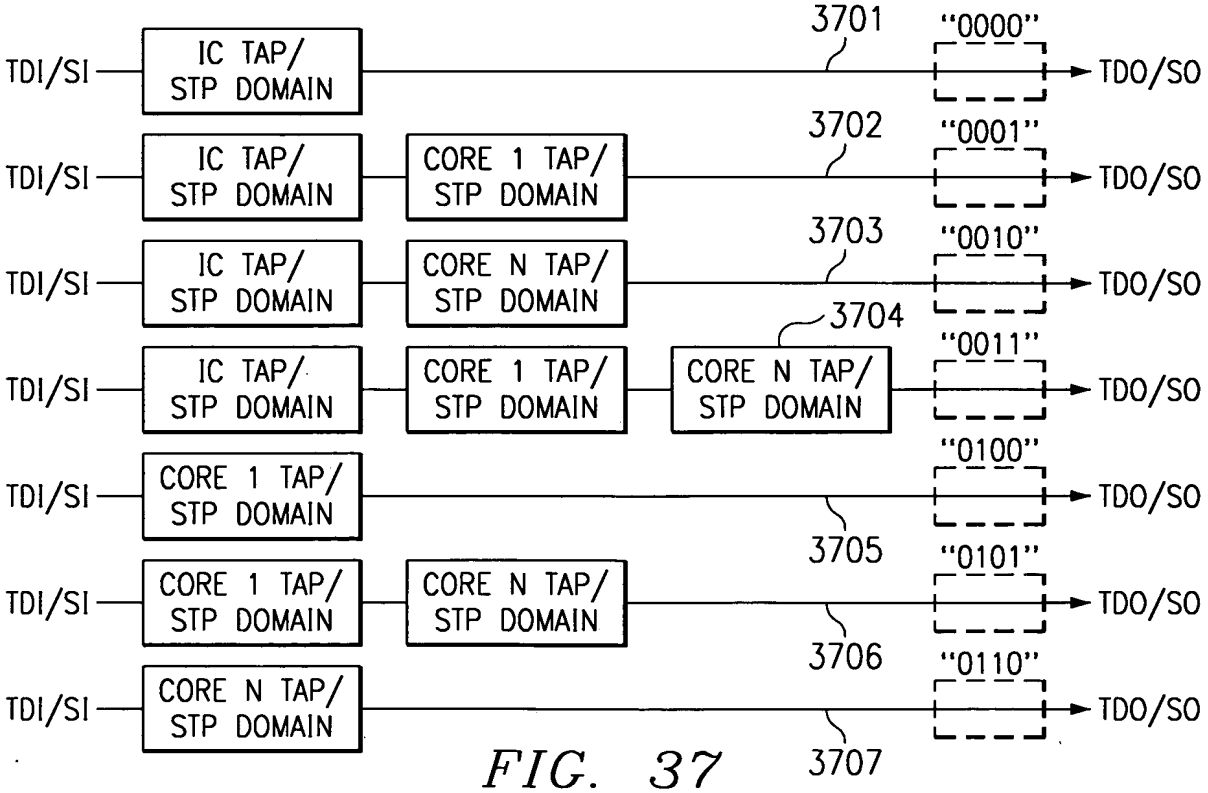

3701
"0000"
TDI/SI
IC TAP/ STP DOMAIN
TDO/SO
3702
"0001"
CORE 1 TAP/ STP DOMAIN
3703
"0010"
CORE N TAP/ STP DOMAIN
3704
"0011"
CORE N TAP/ STP DOMAIN
"0100"
3705
"0101"
3706
"0110"
3707

FIG. 37

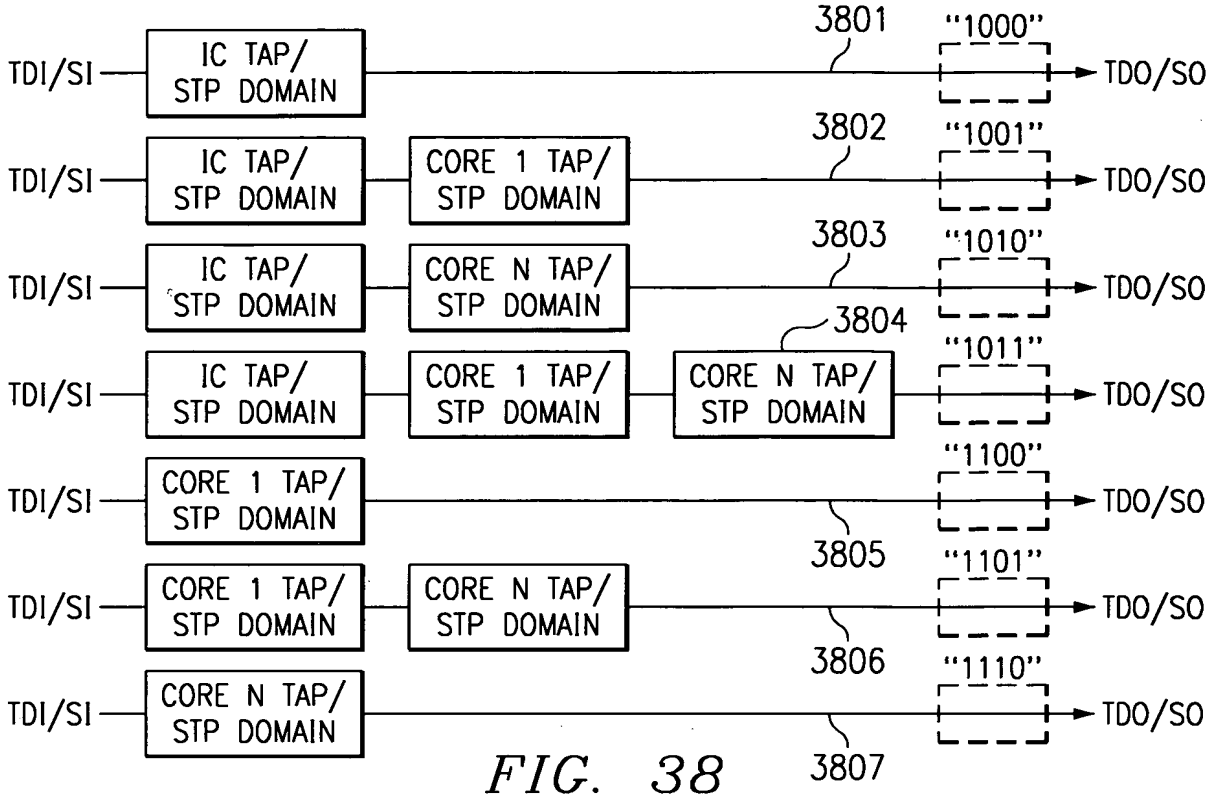

TDI/SI
IC TAP/ STP DOMAIN
CORE 1 TAP/ STP DOMAIN
CORE N TAP/ STP DOMAIN
CORE N TAP/ STP DOMAIN
TDO/SO
3801
3802
3803
3804
3805
3806
3807
"1000"
"1001"
"1010"
"1011"
"1100"
"1101"
"1110"

FIG. 38

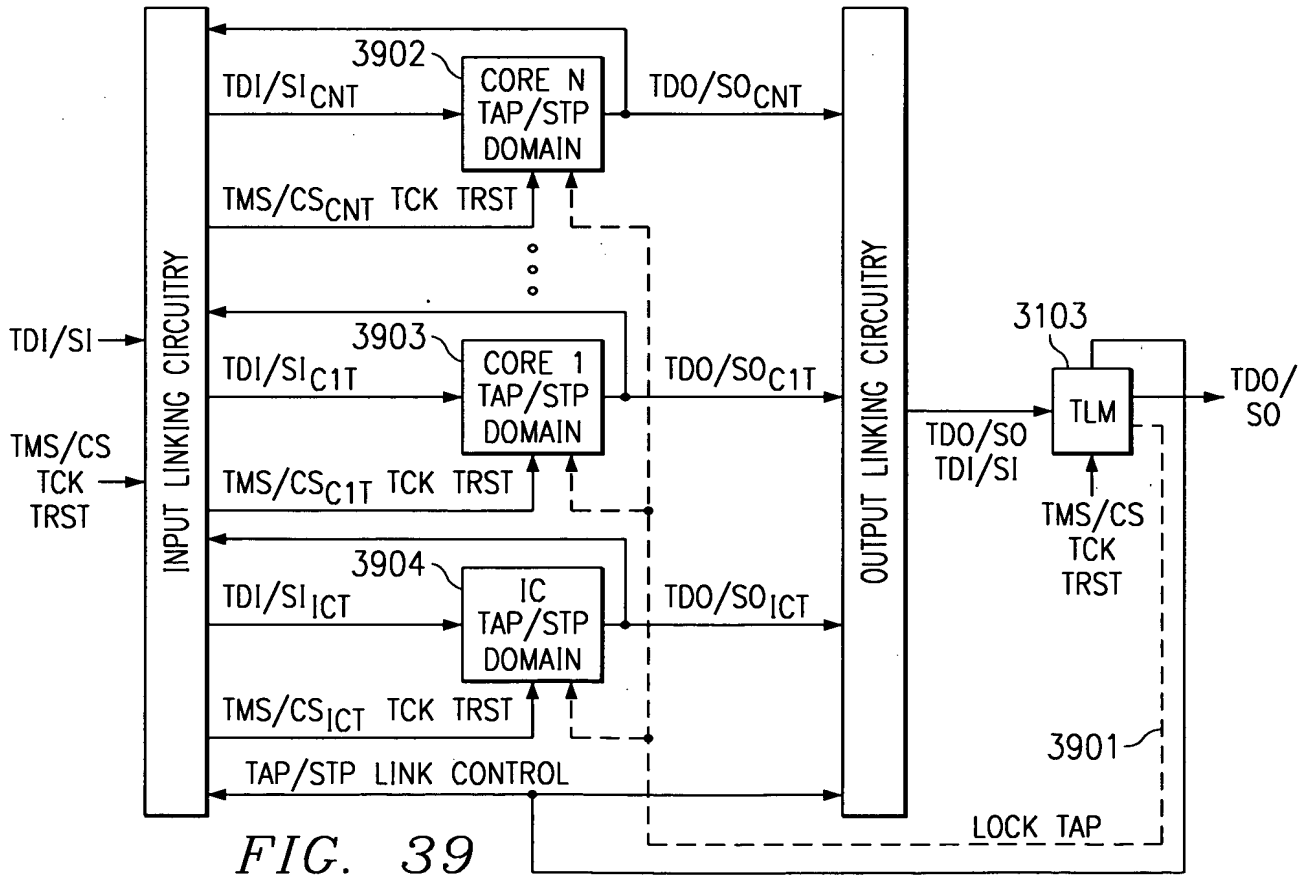

TDI/SI
TMS/CS
TCK
TRST
INPUT LINKING CIRCUITRY
3902
CORE N TAP/STP DOMAIN
TDI/SI CNT
TDO/SO CNT
TMS/CS CNT TCK TRST
3903
CORE 1 TAP/STP DOMAIN
TDI/SI C1T
TDO/SO C1T
TMS/CS C1T TCK TRST
3904
IC TAP/STP DOMAIN
TDI/SI ICT
TDO/SO ICT
TMS/CS ICT TCK TRST
TAP/STP LINK CONTROL
OUTPUT LINKING CIRCUITRY
3103
TLM
TDO/SO
TDI/SI
TMS/CS
TCK
TRST
TDO/ SO
3901
LOCK TAP

FIG. 39

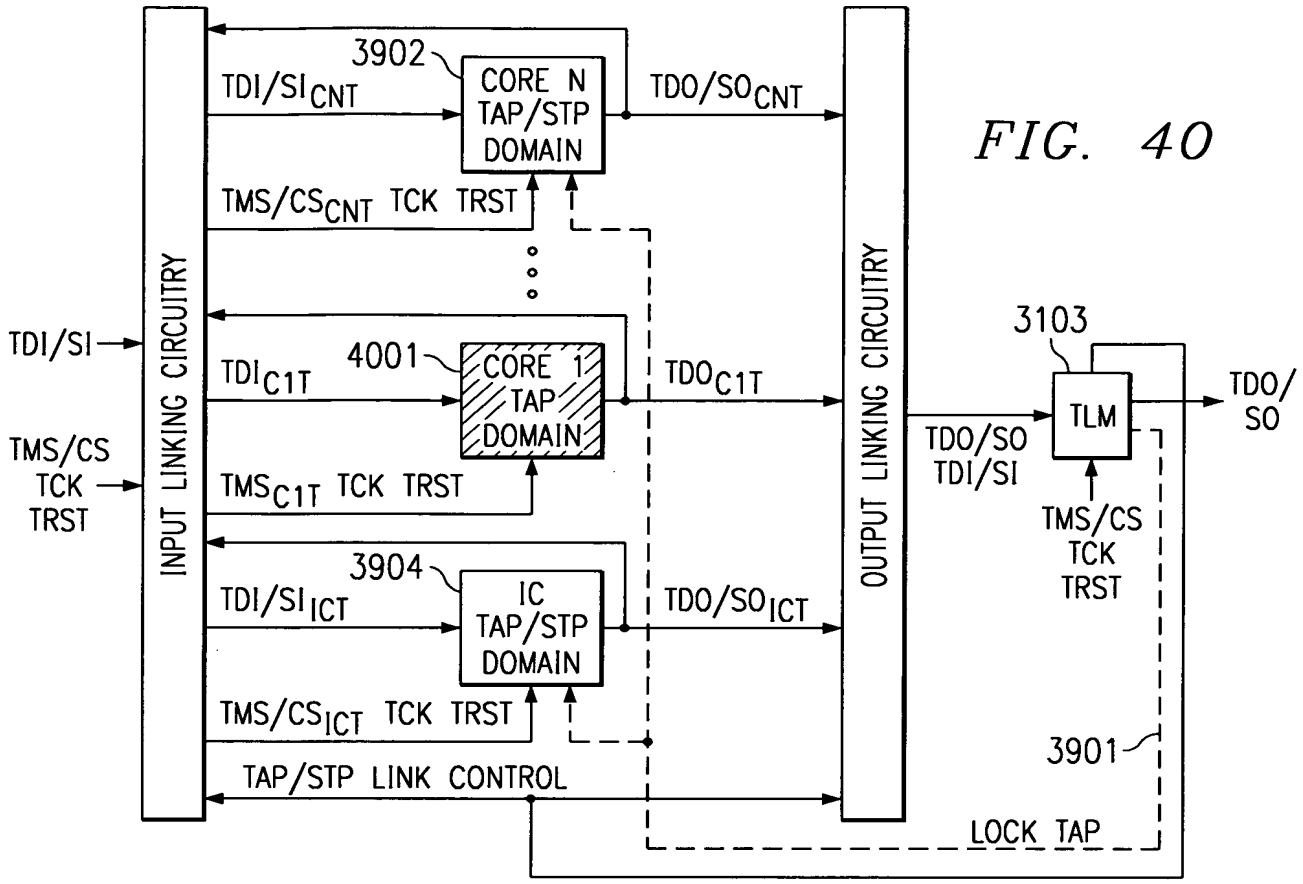

3902
CORE N TAP/STP DOMAIN
TDI/SI$_{CNT}$
TDO/SO$_{CNT}$
TMS/CS$_{CNT}$ TCK TRST
TDI/SI
TMS/CS
TCK
TRST
INPUT LINKING CIRCUITRY
4001
CORE 1 TAP DOMAIN
TDI$_{C1T}$
TDO$_{C1T}$
TMS$_{C1T}$ TCK TRST
3904
IC TAP/STP DOMAIN
TDI/SI$_{ICT}$
TDO/SO$_{ICT}$
TMS/CS$_{ICT}$ TCK TRST
TAP/STP LINK CONTROL
OUTPUT LINKING CIRCUITRY
3103
TLM
TDO/SO
TDI/SI
TMS/CS
TCK
TRST
TDO/SO
3901
LOCK TAP

FIG. 40

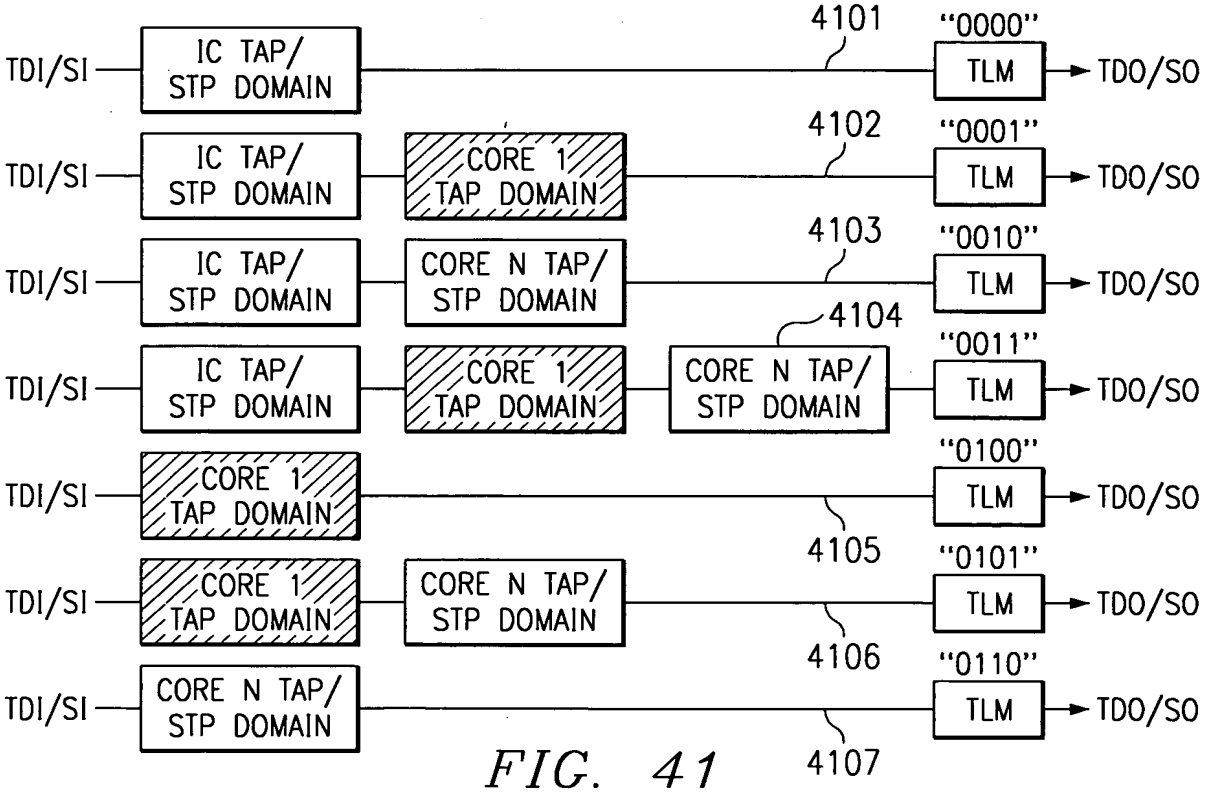

TDI/SI
IC TAP/ STP DOMAIN
CORE 1 TAP DOMAIN
CORE N TAP/ STP DOMAIN
4101
4102
4103
4104
4105
4106
4107
"0000"
"0001"
"0010"
"0011"
"0100"
"0101"
"0110"
TLM
TDO/SO

FIG. 41

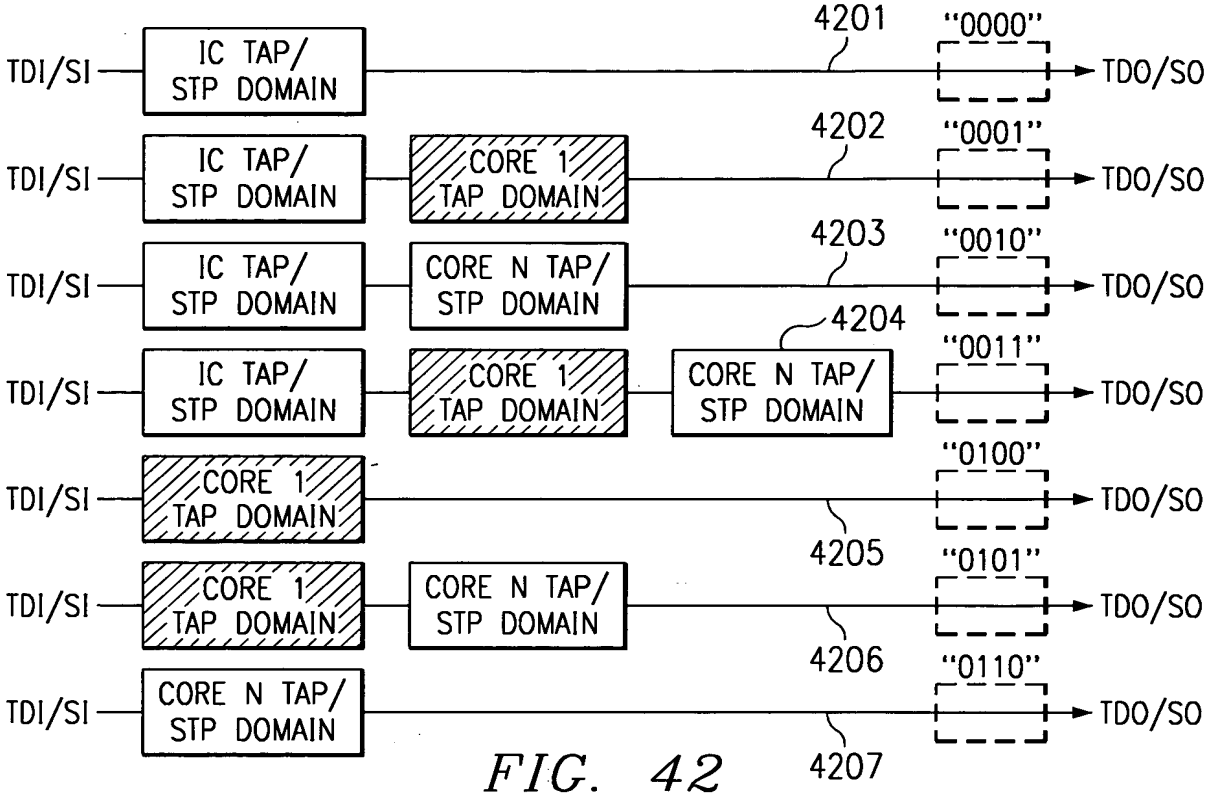

TDI/SI
IC TAP/ STP DOMAIN
CORE 1 TAP DOMAIN
CORE N TAP/ STP DOMAIN
TDO/SO
4201
"0000"
4202
"0001"
4203
"0010"
4204
"0011"
"0100"
4205
"0101"
4206
"0110"
4207

FIG. 42

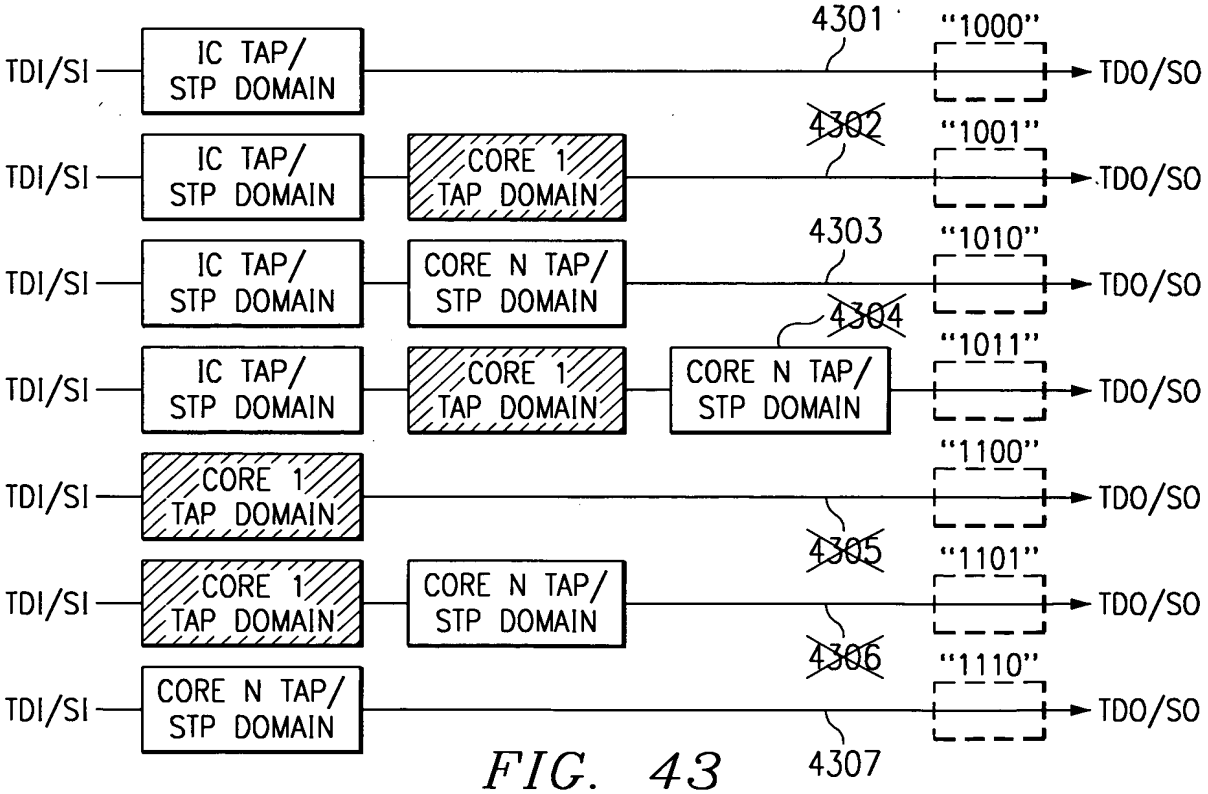

TDI/SI
IC TAP/ STP DOMAIN
CORE 1 TAP DOMAIN
CORE N TAP/ STP DOMAIN
TDO/SO
4301
"1000"
4302
"1001"
4303
"1010"
4304
"1011"
"1100"
4305
"1101"
4306
"1110"
4307

FIG. 43